PROGRAM OUTCOMES (POs)

Engineering Graduates will be able to:

1. **Engineering knowledge**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

2. **Problem analysis**: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

3. **Design/development of solutions**: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

4. **Conduct investigations of complex problems**: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

5. **Modern tool usage**: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

6. **The engineer and society**: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

7. **Environment and sustainability**: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

8. **Ethics**: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

9. **Individual and team work**: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

10. **Communication**: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

11. **Project management and finance**: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
12. **Life-long learning**: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

**The Programme Educational Objectives (PEOs) are,**

1. To equip the graduates to have an in-depth knowledge along with new technical ideas, to analyse and evaluate the potential engineering problems and to contribute to the research and development in the core areas by using modern engineering and IT tools.
2. To demonstrate self – management and teamwork in a collaborative and multidisciplinary arena
3. To inculcate good professional practices with a responsibility to contribute to sustainable development of society.
4. To have a zeal for improving technical competency by continuous and corrective learning.

**The Programme Specific Objectives (PSOS) are,**

1. To design and develop VLSI circuits to optimise power and area requirements, free from faults and dependencies by modelling, simulation and testing.
2. To develop VLSI systems by learning advanced algorithms, architectures and software – hardware co – design.
3. To communicate engineering concepts effectively by exhibiting high standards of technical presentations and scientific documentations.

**MAPPING OF PROGRAMME EDUCATIONAL OBJECTIVES WITH PROGRAMME OUTCOMES:**

A broad relation between the Programme Educational Objectives (PEO) and the Program Outcomes (PO) is given in the following table.

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ANNA UNIVERSITY, CHENNAI
AFFILIATED INSTITUTIONS
M.E. VLSI DESIGN
REGULATIONS – 2017
CHOICE BASED CREDIT SYSTEM
CURRICULA AND SYLLABI

SEMESTER I

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**TOTAL NO. OF CREDITS:** 70

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## PROFESSIONAL ELECTIVES (PE)*

### SEMESTER II

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OBJECTIVES:
The main objective of this course is to demonstrate various analytical skills in applied mathematics and extensive experience with the tactics of problem solving and logical thinking applicable in electronics engineering. This course also will help the students to identify, formulate, abstract, and solve problems in electrical engineering using mathematical tools from a variety of mathematical areas, including fuzzy logic, matrix theory, probability, dynamic programming and queuing theory.

UNIT I  Fuzzy Logic
Classical logic – Multivalued logics – Fuzzy propositions – Fuzzy quantifiers.

UNIT II  Matrix Theory
Cholesky decomposition - Generalized Eigenvectors - Canonical basis - QR factorization - Least squares method - Singular value decomposition.

UNIT III  Probability and Random Variables

UNIT IV  Dynamic Programming

UNIT V  Queueing Models

TOTAL: 60 PERIODS

OUTCOMES:
After completing this course, students should demonstrate competency in the following skills:

- Concepts of fuzzy sets, knowledge representation using fuzzy rules, fuzzy logic, fuzzy propositions and fuzzy quantifiers and applications of fuzzy logic.
- Apply various methods in matrix theory to solve system of linear equations.
- Computation of probability and moments, standard distributions of discrete and continuous random variables and functions of a random variable.
- Conceptualize the principle of optimality and sub-optimization, formulation and computational procedure of dynamic programming
- Exposing the basic characteristic features of a queuing system and acquire skills in analyzing queuing models.
- Using discrete time Markov chains to model computer systems.

REFERENCES:
AP5151 ADVANCED DIGITAL SYSTEM DESIGN

OBJECTIVES:

- To introduce methods to analyze and design synchronous and asynchronous sequential circuits
- To introduce the architectures of programmable devices
- To introduce design and implementation of digital circuits using programming tools

UNIT I SEQUENTIAL CIRCUIT DESIGN

Analysis of clocked synchronous sequential circuits and modeling- State diagram, state table, state table assignment and reduction-Design of synchronous sequential circuits design of iterative circuits-ASM chart and realization using ASM

UNIT II ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN

Analysis of asynchronous sequential circuit – flow table reduction-races-state assignment-transition table and problems in transition table- design of asynchronous sequential circuit-Static, dynamic and essential hazards – data synchronizers – mixed operating mode asynchronous circuits – designing vending machine controller

UNIT III FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS


UNIT IV SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES

Programming logic device families – Designing a synchronous sequential circuit using PLA/PAL – Realization of finite state machine using PLD – FPGA – Xilinx FPGA-Xilinx 4000

UNIT V SYSTEM DESIGN USING VERILOG


TOTAL : 45 PERIODS

OUTCOMES:

At the end of the course, the student should be able to:

- Analyze and design sequential digital circuits
- Identify the requirements and specifications of the system required for a given application
- Design and use programming tools for implementing digital circuits of industry standards

REFERENCES:

2. M.D.Ciletti , Modeling, Synthesis and Rapid Prototyping with the Verilog HDL, Prentice Hall, 1999
OBJECTIVES:
- This course deals comprehensively with all aspects of transistor level design of all the digital building blocks common to all CMOS microprocessors, DPSs, network processors, digital backend of all wireless systems etc.
- The focus will be on the transistor level design and will address all important issues related to size, speed and power consumption. The units are classified according to the important building and will introduce the principles and design methodology in terms of the dominant circuit choices, constraints and performance measures.

UNIT I MOS TRANSISTOR PRINCIPLES AND CMOS INVERTER
MOS(FET) Transistor Characteristic under Static and Dynamic Conditions, MOS Transistor Secondary Effects, Process Variations, Technology Scaling, Internet Parameter and electrical wise models CMOS Inverter - Static Characteristic, Dynamic Characteristic, Power, Energy, and Energy Delay parameters.

UNIT II COMBINATIONAL LOGIC CIRCUITS

UNIT III SEQUENTIAL LOGIC CIRCUITS
Static Latches and Registers, Dynamic Latches and Registers, Timing Issues, Pipelines, Pulse and sense amplifier based Registers, Nonbistable Sequential Circuits.

UNIT IV ARITHMETIC BUILDING BLOCKS AND MEMORY ARCHITECTURES
Data path circuits, Architectures for Adders, Accumulators, Multipliers, Barrel Shifters, Speed and Area Tradeoffs, Memory Architectures, and Memory control circuits.

UNIT V INTERCONNECT AND CLOCKING STRATEGIES

OUTCOMES:
At the end of the course, the student should be able to:
- Carry out transistor level design of the most important building blocks used in digital CMOS VLSI circuits.
- Discuss design methodology of arithmetic building block
- Analyze tradeoffs of the various circuit choices for each of the building block.

REFERENCES:
OBJECTIVES:
- To familiarize the concept of DSP and DSP algorithms.
- Introduction to Multirate systems and finite wordlength effects
- To know about the basic DSP processor architectures and the synthesis of the processing elements

UNIT I INTRODUCTION TO DSP INTEGRATED CIRCUITS
Introduction to Digital signal processing, Sampling of analog signals, Selection of sample frequency, Signal- processing systems, Frequency response, Transfer functions, Signal flow graphs, Filter structures, Adaptive DSP algorithms, DFT-The Discrete Fourier Transform, FFT Algorithm, Image coding, Discrete cosine transforms, Standard digital signal processors, Application specific ICs for DSP, DSP systems, DSP system design, Integrated circuit design.

UNIT II DIGITAL FILTERS AND FINITE WORD LENGTH EFFECTS
FIR filters, FIR filter structures, FIR chips, IIR filters, Specifications of IIR filters, Mapping of analog transfer functions, Mapping of analog filter structures, Multi rate systems, Interpolation with an integer factor L, Sampling rate change with a ratio L/M, Multi rate filters. Finite word length effects - Parasitic oscillations, Scaling of signal levels, Round-off noise, Measuring round-off noise, Coefficient sensitivity, Sensitivity and noise.

UNIT III DSP ARCHITECTURES
DSP system architectures, Standard DSP architecture-Harvard and Modified Harvard architecture. Ideal DSP architectures, Multiprocessors and multi computers, Systolic and Wave front arrays, Shared memory architectures.

UNIT IV SYNTHESIS OF DSP ARCHITECTURES
Synthesis: Mapping of DSP algorithms onto hardware, Implementation based on complex PEs, Shared memory architecture with Bit – serial PEs. Combinational & sequential networks- Storage elements – clocking of synchronous systems, Asynchronous systems -FSM

UNIT V ARITHMETIC UNIT AND PROCESSING ELEMENTS
Conventional number system, Redundant Number system, Residue Number System, Bit-parallel and Bit-Serial arithmetic, Digit Serial arithmetic, CORDIC Algorithm, Basic shift accumulator, Reducing the memory size, Complex multipliers, Improved shift-accumulator. Case Study: DCT and FFT processor

OUTCOMES:
- Get to know about the Digital Signal Processing concepts and its algorithms
- Get an idea about finite word length effects in digital filters
- Concept behind multi rate systems is understood.
- Get familiar with the DSP processor architectures and how to perform synthesis of processing elements

REFERENCES:
OBJECTIVES:
The students should be made to:
- Learn VLSI Design methodologies
- Understand VLSI design automation tools
- Study modelling and simulation

UNIT I  INTRODUCTION TO VLSI DESIGN FLOW  9
Introduction to VLSI Design methodologies, Basics of VLSI design automation tools, Algorithmic
Graph Theory and Computational Complexity, Tractable and Intractable problems, General purpose
methods for combinatorial optimization.

UNIT II  LAYOUT, PLACEMENT AND PARTITIONING  9
Layout Compaction, Design rules, Problem formulation, Algorithms for constraint graph compaction,
Placement and partitioning, Circuit representation, Placement algorithms, Partitioning

UNIT III  FLOOR PLANNING AND ROUTING  9
Floor planning concepts, Shape functions and floorplan sizing, Types of local routing problems, Area
routing, Channel routing, Global routing, Algorithms for global routing.

UNIT IV  SIMULATION AND LOGIC SYNTHESIS  9
Simulation, Gate-level modeling and simulation, Switch-level modeling and simulation, Combinational
Logic Synthesis, Binary Decision Diagrams, Two Level Logic Synthesis.

UNIT V  HIGH LEVEL SYNTHESIS  9
Hardware models for high level synthesis, internal representation, allocation, assignment and
scheduling, scheduling algorithms, Assignment problem, High level transformations.

TOTAL: 45 PERIODS

OUTCOMES:
At the end of this course, the students should be able to:
- Outline floor planning and routing
- Explain Simulation and Logic Synthesis
- Discuss the hardware models for high level synthesis

REFERENCES:
   Scientific 1999.
OBJECTIVES

- To study MOS devices modelling and scaling effects.
- To familiarize the design of single stage and multistage MOS amplifier and analysis their frequency responses.
- To study the different design parameters in designing voltage reference and OPAMP circuits.

UNIT I MOSFET METRICS

Simple long channel MOSFET theory – SPICE Models – Technology trend, Need for Analog design - Sub-micron transistor theory, Short channel effects, Narrow width effect, Drain induced barrier lowering, Sub-threshold conduction, Reliability, Digital metrics, Analog metrics, Small signal parameters, Unity Gain Frequency, Miller’s approximation

UNIT II SINGLE STAGE AND TWO STAGE AMPLIFIERS

Single Stage Amplifiers – Common source amplifier with resistive load, diode load, constant current load, Source degeneration Source follower, Input and output impedance, Common gate amplifier - Differential Amplifiers – differential and common mode response, Input swing, gain, diode load and constant current load - Basic Two Stage Amplifier, Cut-off frequency, poles and zeros

UNIT III FREQUENCY RESPONSE OF SINGLE STAGE AND TWO STAGE AMPLIFIERS


UNIT IV CURRENT MIRRORS AND REFERENCE CIRCUITS

Cascode, Negative feedback, Wilson, Regulated cascode, Bandgap voltage reference, Constant Gm biasing, supply and temperature independent reference, curvature compensation, trimming, Effect of transistor mismatch in analog design

UNIT V OP AMPS

Gilbert cell and applications, Basic two stage OPAMP, two-pole system response, common mode and differential gain, Frequency response of OPAMP, CMFB circuits, slew rate, power supply rejection ratio, random offset, systematic offset, Noise, Output stage, OTA and OPAMP circuits - Low voltage OPAMP

OUTCOMES:

- To design MOS single stage, multistage amplifiers and OPAMP for desired frequencies
- Analyze Stability, frequency response, and Noise in MOS amplifiers

REFERENCES:

OBJECTIVES:
The laboratory based study for the entire program is clubbed under three categories. One is the FPGA based design methodology; the second is the simulation of analog building blocks, and analog and digital CAD design flow. Experiments pertaining to the former two topics are covered in this lab course and those pertaining to the latter will be covered in VLSI Design Lab II.
FPGAs are important platform used throughout the industry both in their own right in building complete systems. They are also used as validation/verification platforms prior to undertaking cost and time intensive design and fabrication of custom VLSI designs. Starting from high level design entry in the form VHDL/Verilog codes, the students will be carrying out complete hardware level FPGA validation of important digital algorithms. In addition, exercises on the SPICE simulation of the basic CMOS analog building blocks will be carried out.

EXPERIMENTS:
2. Test vector generation and timing analysis of sequential and combinational logic design realized using HDL languages.
3. FPGA real time programming and I/O interfacing.
4. Interfacing with Memory modules in FPGA Boards.
5. Verification of design functionality implemented in FPGA by capturing the signal in DSO.
6. Real time application development.
7. Design Entry Using VHDL or Verilog examples for Digital circuit descriptions using HDL languages sequential, concurrent statements and structural description.

TOTAL : 60 PERIODS

OUTCOMES:
At the end of the course, the student should be able to: After completing this course, given a digital system specification, the student should be able to map it onto FPGA platform and carry out a series of validations design starting from design entry to hardware testing. In addition, the student also will be able to design and carry out time domain and frequency domain simulations of simple analog building blocks, study the pole zero behaviors of feedback based circuits and compute the input/output impedances.

OBJECTIVES:
The students should be made to:
- Understand logic fault models
- Learn test generation for sequential and combinational logic circuits

UNIT I TESTING AND FAULT MODELLING

UNIT II TEST GENERATION
Test generation for combinational logic circuits – Testable combinational logic circuit design – Test generation for sequential circuits – design of testable sequential circuits.
UNIT III DESIGN FOR TESTABILITY
Design for Testability – Ad-hoc design – generic scan based design – classical scan based design– system level DFT approaches.

UNIT IV SELF – TEST AND TEST ALGORITHMS

UNIT V FAULT DIAGNOSIS
Logical Level Diagnosis – Diagnosis by UUT reduction – Fault Diagnosis for Combinational Circuits– Self-checking design – System Level Diagnosis.

TOTAL: 45 PERIODS

OUTCOMES:
At the end of this course, the students should be able to:
- Prepare design for testability
- Discuss test algorithms
- Explain fault diagnosis

REFERENCES:

VL5291 VLSI SIGNAL PROCESSING L T P C
3 0 0 3

OBJECTIVES:
- To introduce techniques for altering the existing DSP structures to suit VLSI implementations.
- To introduce efficient design of DSP architectures suitable for VLSI

UNIT I PIPELINING AND PARALLEL PROCESSING OF DIGITAL FILTERS
Introduction to DSP systems – Typical DSP algorithms, Data flow and Dependence graphs – critical path, Loop bound, iteration bound, Longest path matrix algorithm, Pipelining and Parallel processing of FIR filters, Pipelining and Parallel processing for low power.

UNIT II ALGORITHMIC STRENGTH REDUCTION TECHNIQUE I

UNIT III ALGORITHMIC STRENGTH REDUCTION -II
**UNIT IV**  
BIT-LEVEL ARITHMETIC ARCHITECTURES  
9
Bit-level arithmetic architectures – parallel multipliers with sign extension, parallel carry-ripple and carry-save multipliers, Design of Lyon’s bit-serial multipliers using Horner’s rule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner’s rule for precision improvement, Distributed Arithmetic fundamentals and FIR filters

**UNIT V**  
NUMERICAL STRENGTH REDUCTION, WAVE AND ASYNCHRONOUS PIPELINING  
9

**OUTCOME:**
- Ability to modify the existing or new DSP architectures suitable for VLSI.

**REFERENCES:**

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**VL5202**  
LOW POWER VLSI DESIGN  
L T P C
3 0 0 3

**OBJECTIVES:**
- Identify sources of power in an IC.
- Identify the power reduction techniques based on technology independent and technology dependent
- Power dissipation mechanism in various MOS logic style.
- Identify suitable techniques to reduce the power dissipation.
- Design memory circuits with low power dissipation.

**UNIT I**  
POWER DISSIPATION IN CMOS  
9

**UNIT II**  
POWER OPTIMIZATION  
9
Logic level power optimization – Circuit level low power design – Standard Adder Cells, CMOS Adders Architectures-BiCMOS adders - Low Voltage Low Power Design Techniques, Current Mode Adders -Types Of Multiplier Architectures, Braun, Booth and Wallace Tree Multipliers and their performance comparison

**UNIT III**  
DESIGN OF LOW POWER CMOS CIRCUITS  
9
Computer arithmetic techniques for low power system – low voltage low power static Random access and dynamic Random access memories – low power clock, Inter connect and layout design – Advanced techniques – Special techniques.
UNIT IV       POWER ESTIMATION
Power Estimation techniques – logic power estimation – Simulation power analysis – Probabilistic
power analysis.

UNIT V       SYNTHESIS AND SOFTWARE DESIGN FOR LOW POWER
Synthesis for low power – Behavioral level transform – software design for low power.

TOTAL: 45 PERIODS

OUTCOMES:
- The student will get to know the basics and advanced techniques in low power design which is
  a hot topic in today’s market where the power plays major role.
- The reduction in power dissipation by an IC earns a lot including reduction in size, cost and etc.

REFERENCES:

VL5211       VLSI DESIGN LABORATORY II
L T P C
0 0 4 2

OBJECTIVE:
The focus of this course the CAD based VLSI design flow. The entire VLSI design industry makes use
of this design flow in some or the other. Proficiency and familiarity with the various stages of a
typical “state of this design flow is a prerequisite for any student who wishes to be apart of either the
industry or their search in VLSI over one full semester exposure to various stages of a typical state of
the art CAD VLSI tool be provided by various experiments designed to bring out the key aspects of
simulation, and power and clock routing modules. ASIC RTL realization of an available open source
MCU

EXPERIMENTS:
To synthesize and understand the Boolean optimization in synthesis. Static timing analyses
procedures and constraints. Critical path considerations. Scan chain insertion, Floor planning, Routing
and Placement procedures. Power planning, Layout generation, LVS and back annotation, Total
power estimate. Analog circuit simulation. Simulation of logic gates, Current mirrors, Current sources,
Differential amplifier in Spice.
Layout generations, LVS, Back annotation

TOTAL: 60 PERIODS

OUTCOMES:
The student would have hands on experience in the carrying out a complete VLSI based experiments
using / CADENCE/ TANNER/ Mentor/Synopsis
In this course, students will develop their scientific and technical reading and writing skills that they need to understand and construct research articles. A term paper requires a student to obtain information from a variety of sources (i.e., Journals, dictionaries, reference books) and then place it in logically developed ideas. The work involves the following steps:

1. Selecting a subject, narrowing the subject into a topic
2. Stating an objective.
3. Collecting the relevant bibliography (atleast 15 journal papers)
4. Preparing a working outline.
5. Studying the papers and understanding the authors contributions and critically analysing each paper.
6. Preparing a working outline
7. Linking the papers and preparing a draft of the paper.
8. Preparing conclusions based on the reading of all the papers.
9. Writing the Final Paper and giving final Presentation

Please keep a file where the work carried out by you is maintained.
Activities to be carried out by you is maintained.

<table>
<thead>
<tr>
<th>Activity</th>
<th>Instructions</th>
<th>Submission week</th>
<th>Evaluation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Selection of area of interest and Topic</td>
<td>You are requested to select an area of interest, topic and state an objective</td>
<td>2nd week</td>
<td>3 % Based on clarity of thought, current relevance and clarity in writing</td>
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<tr>
<td>Stating an Objective</td>
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<tr>
<td>Collecting Information about your area &amp; topic</td>
<td>1. List 1 Special Interest Groups or professional society</td>
<td>3rd week</td>
<td>3% (the selected information must be area specific and of international and national standard)</td>
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<td>2. List 2 journals</td>
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<td>3. List 2 conferences, symposia or workshops</td>
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<td>4. List 1 thesis title</td>
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<td>5. List 3 web presences (mailing lists, forums, news sites)</td>
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<td>6. List 3 authors who publish regularly in your area</td>
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<td>7. Attach a call for papers (CFP) from your area</td>
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<tr>
<td>Collection of Journal papers in the topic in the context of the objective – collect 20 &amp; then filter</td>
<td>You have to provide a complete list of references you will be using- Based on your objective -Search various digital libraries and Google Scholar</td>
<td>4th week</td>
<td>6% (the list of standard papers and reason for selection)</td>
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<td></td>
<td>• When picking papers to read - try to:</td>
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<td>• Pick papers that are related to each other in some ways and/or that are in the same field so that you can write a meaningful survey out of them,</td>
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<td>• Favour papers from well-known journals and conferences,</td>
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</table>
- Favour “first” or “foundational” papers in the field (as indicated in other people’s survey paper),
- Favour more recent papers,
- Pick a recent survey of the field so you can quickly gain an overview,
- Find relationships with respect to each other and to your topic area (classification scheme/categorization)
- Mark in the hard copy of papers whether complete work or section/sections of the paper are being considered

<table>
<thead>
<tr>
<th>Reading and notes for first 5 papers</th>
<th>Reading Paper Process</th>
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</thead>
<tbody>
<tr>
<td></td>
<td>For each paper form a Table answering the following questions:</td>
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<tr>
<td></td>
<td>What is the main topic of the article?</td>
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<tr>
<td></td>
<td>What was/were the main issue(s) the author said they want to discuss?</td>
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<tr>
<td></td>
<td>Why did the author claim it was important?</td>
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<td></td>
<td>How does the work build on other’s work, in the author’s opinion?</td>
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<td></td>
<td>What simplifying assumptions does the author claim to be making?</td>
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<td></td>
<td>What did the author do?</td>
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<td></td>
<td>How did the author claim they were going to evaluate their work and compare it to others?</td>
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<tr>
<td></td>
<td>What did the author say were the limitations of their research?</td>
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<tr>
<td></td>
<td>What did the author say were the important directions for future research?</td>
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<td></td>
<td>Conclude with limitations/issues not addressed by the paper (from the perspective of your survey)</td>
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</tbody>
</table>

5th week 8% (the table given should indicate your understanding of the paper and the evaluation is based on your conclusions about each paper)

<table>
<thead>
<tr>
<th>Reading and notes for next 5 papers</th>
<th>Repeat Reading Paper Process</th>
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</table>
|                                     | 6th week 8% (the table given should indicate your understanding of the paper and the evaluation is based on your conclusions about each paper)

<table>
<thead>
<tr>
<th>Reading and notes for final 5 papers</th>
<th>Repeat Reading Paper Process</th>
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<tbody>
<tr>
<td></td>
<td>7th week 8% (the table given should indicate your understanding of the paper and the evaluation is based on your conclusions about each paper)</td>
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<tr>
<td>Task</td>
<td>Description</td>
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<tr>
<td>Draft outline 1 and Linking papers</td>
<td>Prepare a draft Outline, your survey goals, along with a classification / categorization diagram</td>
</tr>
<tr>
<td>Abstract</td>
<td>Prepare a draft abstract and give a presentation</td>
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<tr>
<td>Introduction Background</td>
<td>Write an introduction and background sections</td>
</tr>
<tr>
<td>Sections of the paper</td>
<td>Write the sections of your paper based on the classification / categorization diagram in keeping with the goals of your survey</td>
</tr>
<tr>
<td>Your conclusions</td>
<td>Write your conclusions and future work</td>
</tr>
<tr>
<td>Final Draft</td>
<td>Complete the final draft of your paper</td>
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<tr>
<td>Seminar</td>
<td>A brief 15 slides on your paper</td>
</tr>
</tbody>
</table>

**TOTAL : 30 PERIODS**

**VL5301 ANALOG TO DIGITAL INTERFACES**

**OBJECTIVES**
- To understand the importance of sampling the input analog signal for digitization and enabling circuit architectures
- To understand the principles of Analog to Digital and Digital to Analog conversion of signals.
- To understand the importance of calibration techniques for achieving precision during data conversion

**UNIT I  SAMPLE AND HOLD CIRCUITS**
Sampling switches, Conventional open loop and closed loop sample and hold architecture, Open loop architecture with miller compensation, multiplexed input architectures, recycling architecture switched capacitor architecture.
UNIT II SWITCHED CAPACITOR CIRCUITS AND COMPARATORS 9
Switched-capacitor amplifiers, switched capacitor integrator, switched capacitor common mode feedback. Single stage amplifier as comparator, cascaded amplifier stages as comparator, latched comparators.

UNIT III DIGITAL TO ANALOG CONVERSION 9
Performance metrics, reference multiplication and division, switching and logic functions in DAC, Resistor ladder DAC architecture, current steering DAC architecture.

UNIT IV ANALOG TO DIGITAL CONVERSION 9
Performance metric, Flash architecture, Pipelined Architecture, Successive approximation architecture, Time interleaved architecture.

UNIT V PRECISION TECHNIQUES 9
Comparator offset cancellation, Op Amp offset cancellation, Calibration techniques, range overlap and digital correction.

TOTAL: 45 PERIODS

OUTCOMES:
- To be able to design Analog to Digital and Digital to Analog data converters based on data precision requirements

REFERENCE:

VL5001 DEVICE MODELING - I L T P C
3 0 0 3

OBJECTIVES
- To study the MOS capacitors and to model MOS Transistors
- To understand the various CMOS design parameters and their impact on performance of the device.
- To study the device level characteristics of BJT transistors

UNIT I MOS CAPACITORS 9
Surface Potential: Accumulation, Depletion, and Inversion, Electrostatic Potential and Charge Distribution in Silicon, Capacitances in an MOS Structure, Polysilicon-Gate Work Function and Depletion Effects, MOS under Nonequilibrium and Gated Diodes, Charge in Silicon Dioxide and at the Silicon–Oxide Interface, Effect of Interface Traps and Oxide Charge on Device Characteristics, High-Field Effects, Impact Ionization and Avalanche Breakdown, Band-to-Band Tunneling, Tunneling into and through Silicon Dioxide, Injection of Hot Carriers from Silicon into Silicon Dioxide, High-Field Effects in Gated Diodes, Dielectric Breakdown

UNIT II MOSFET DEVICES 9
Long-Channel MOSFETs, Drain-Current Model, MOSFET I–V Characteristics, Subthreshold Characteristics, Substrate Bias and Temperature Dependence of Threshold Voltage, MOSFET Channel Mobility, MOSFET Capacitances and Inversion-Layer Capacitance Effect, Short-Channel MOSFETs, Short-Channel Effect, Velocity Saturation and High-Field Transport Channel Length Modulation, Source–Drain Series Resistance, MOSFET Degradation and Breakdown at High Fields
UNIT III  CMOS DEVICE DESIGN

UNIT IV  CMOS PERFORMANCE FACTORS

UNIT V  BIPOLAR DEVICES

OUTCOMES:
To design and model MOSFET and BJT devices to desired specifications.

REFERENCES:

TOTAL: 45 PERIODS

VL5002  RF IC DESIGN  L T P C
3 0 0 3

OBJECTIVES:
- To study the various impedance matching techniques used in RF circuit design.
- To understand the functional design aspects of LNAs, Mixers, PLLs and VCO.
- To understand frequency synthesis.

UNIT I  IMPEDANCE MATCHING IN AMPLIFIERS
UNIT II AMPLIFIER DESIGN 9
Noise characteristics of MOS devices, Design of CG LNA and inductor degenerated LNAs. Principles of RF Power Amplifiers design.

UNIT III ACTIVE AND PASSIVE MIXERS 9

UNIT IV OSCILLATORS 9
LC Oscillators, Voltage Controlled Oscillators, Ring oscillators, Delay Cells, tuning range in ring oscillators, Tuning in LC oscillators, Tuning sensitivity, Phase Noise in oscillators, sources of phase noise.

UNIT V PLL AND FREQUENCY SYNTHESIZERS 9
Phase Detector/Charge Pump, Analog Phase Detectors, Digital Phase Detectors, Frequency Dividers, Loop Filter Design, Phase Locked Loops, Phase noise in PLL, Loop Bandwidth, Basic Integer-N frequency synthesizer, Basic Fractional-N frequency synthesizer

TOTAL: 45 PERIODS

OUTCOMES:
To understand the principles of operation of an RF receiver front end and be able to design and apply constraints for LNAs, Mixers and Frequency synthesizers.

REFERENCES:

VL5003 DESIGN OF ANALOG FILTERS AND SIGNAL CONDITIONING L T P C CIRCUITS 3 0 0 3

OBJECTIVE:
This course deals with CMOS circuit design of various Analog Filter architectures. The required signal conditioning techniques in a Mixed signal IC environment are also dealt in this course.

UNIT I FILTER TOPOLOGIES 9
The Bilinear Transfer Function - Active RC Implementation, Transconductor-C Implementation, Switched Capacitor Implementation, Biquadratic Transfer Function, Active RC implementation, Switched capacitor implementation, High Q, Q peaking and instability, Transconductor-C Implementation, the Digital Biquad.

UNIT II INTEGRATOR REALIZATION 9
UNIT III  SWITCHED CAPACITOR FILTER REALIZATION  9
Switched capacitor Technique, Biquadratic SC Filters, SC N-path filters, Finite gain and bandwidth
effects, Layout consideration, Noise in SC Filters.

UNIT IV  SIGNAL CONDITIONING TECHNIQUES  9
Interference types and reduction, Signal circuit grounding, Shield grounding, Signal conditioners for
capacitive sensors, Noise and Drift in Resistors, Layout Techniques.

UNIT V  SIGNAL CONDITIONING CIRCUITS  9
Isolation Amplifiers, Chopper and Low Drift Amplifiers, Electrometer and Transimpendance Amplifiers,
Charge Amplifiers, Noise in Amplifiers

TOTAL : 45 PERIODS

OUTCOMES:
The student will apply the operational and design principles for all the important active analog filter
configurations. The student also will gain working knowledge of signal conditioning techniques and the
necessary guide lines in a Mixed signal IC environment.

REFERENCES:
1. Ramson Pallas-Areny, John G. Webster “Sensors and Signal Conditioning” , A wiley Inter
3. Schauman, Xiao and Van Valkenburg, “Design of Analog Filters”, Oxford University Press,
2009.

VL5004  NANO SCALE DEVICES  L T P C
3 0 0 3

OBJECTIVES
- To introduce novel MOSFET devices and understand the advantages of multi-gate devices
- To introduce the concepts of nanoscale MOS transistor and their performance characteristics
- To study the various nano scaled MOS transistors

UNIT I  INTRODUCTION TO NOVEL MOSFETS  9
MOSFET scaling, short channel effects - channel engineering - source/drain engineering - high k
dielectric - copper interconnects - strain engineering, SOI MOSFET, multigate transistors – single gate
voltage – inter subband scattering, multigate technology – mobility – gate stack

UNIT II  PHYSICS OF MULTIGATE MOS SYSTEMS  9
MOS Electrostatics – 1D – 2D MOS Electrostatics, MOSFET Current-Voltage Characteristics – CMOS
Technology – Ultimate limits, double gate MOS system – gate voltage effect - semiconductor
thickness effect – asymmetry effect – oxide thickness effect – electron tunnel
current – two dimensional confinement, scattering – mobility

UNIT III  NANOWIRE FETS AND TRANSISTORS AT THE MOLECULAR SCALE  9
Silicon nanowire MOSFETs – Evaluation of I-V characteristics – The I-V characteristics for non-
degenerate carrier statistics – The I-V characteristics for degenerate carrier statistics – Carbon
nanotube – Band structure of carbon nanotube – Band structure of graphene – Physical structure of
nanotube – Band structure of nanotube – Carbon nanotube FETs – Carbon nanotube MOSFETs –
Schottky barrier carbon nanotube FETs – Electronic conduction in molecules – General model for
ballistic nano transistors – MOSFETs with 0D, 1D, and 2D channels – Molecular transistors – Single
electron charging – Single electron transistors
UNIT IV  RADIATION EFFECTS  9
Radiation effects in SOI MOSFETs, total ionizing dose effects – single gate SOI – multigate devices, single event effect, scaling effects

UNIT V  CIRCUIT DESIGN USING MULTIGATE DEVICES  9

TOTAL : 45 PERIODS

OUTCOMES
• To design circuits using nano scaled MOS transistors with the physical insight of their functional characteristics

REFERENCES:

AP5072  DSP PROCESSOR ARCHITECTURE AND PROGRAMMING  L T P C
3 0 0 3

OBJECTIVES:
The objective of this course is to provide in-depth knowledge on
• Digital Signal Processor basics
• Third generation DSP Architecture and programming skills
• Advanced DSP architectures and some applications.

UNIT I  FUNDAMENTALS OF PROGRAMMABLE DSPs  9
Multiplier and Multiplier accumulator – Modified Bus Structures and Memory access in PDSPs – Multiple access memory – Multi-port memory – VLIW architecture- Pipelining – Special Addressing modes in P-DSPs – On chip Peripherals.

UNIT II  SPECIAL FUNCTIONS  9
Architecture – Assembly language syntax - Addressing modes – Assembly language Instructions - Pipeline structure, Operation – Block Diagram of DSP starter kit – Application Programs for processing real time signals.

UNIT III  LINEAR PROGRAMMING  9

UNIT IV  ALGEBRAIC EQUATIONS  9
Architecture of ADSP-21XX and ADSP-210XX series of DSP processors- Addressing modes and assembly language instructions – Application programs –Filter design, FFT calculation.
UNIT V  ORDINARY DIFFERENTIAL EQUATIONS  
9  

TOTAL : 45 PERIODS  

OUTCOMES:  
Students should be able to:  
• Become Digital Signal Processor specialized engineer  
• DSP based System Developer  

REFERENCES:  

VL5005  NETWORKS ON CHIP  
L T P C  
3 0 0 3

OBJECTIVES:  
The students should be made to:  
• Understand the concept of network - on - chip  
• Learn router architecture designs  
• Study fault tolerance network - on - chip

UNIT I  INTRODUCTION TO NOC  
9  
Introduction to NoC – OSI layer rules in NoC - Interconnection Networks in Network-on-Chip Network Topologies - Switching Techniques - Routing Strategies - Flow Control Protocol Quality-of-Service Support

UNIT II  ARCHITECTURE DESIGN  
9  

UNIT III  ROUTING ALGORITHM  
9  
Packet routing-Qos, congestion control and flow control – router design – network link design – Efficient and Deadlock-Free Tree-Based Multicast Routing Methods - Path-Based Multicast Routing for 2D and 3D Mesh Networks- Fault-Tolerant Routing Algorithms - Reliable and Adaptive Routing Algorithms

UNIT IV  TEST AND FAULT TOLERANCE OF NOC  
9  
Design-Security in Networks-on-Chips-Formal Verification of Communications in Networks-on-Chips- Test and Fault Tolerance for Networks-on-Chip Infrastructures-Monitoring Services for Networks-on-Chips.
UNIT V
THREE-DIMENSIONAL INTEGRATION OF NETWORK-ON-CHIP


TOTAL: 45 PERIODS

OUTCOMES:
At the end of this course, the students should be able to:

- Compare different architecture design
- Discuss different routing algorithms
- Explain three dimensional networks - on-chip architectures

REFERENCES:

AP5094
SIGNAL INTEGRITY FOR HIGH SPEED DESIGN

OBJECTIVES:
- To identify sources affecting the speed of digital circuits.
- To introduce methods to improve the signal transmission characteristics

UNIT I
SIGNAL PROPAGATION ON TRANSMISSION LINES
Transmission line equations, wave solution, wave vs. circuits, initial wave, delay time, Characteristic impedance , wave propagation, reflection, and bounce diagrams Reactive terminations – L, C , static field maps of micro strip and strip line cross-sections, per unit length parameters, PCB layer stackups and layer/Cu thicknesses, cross-sectional analysis tools, Zo and Td equations for microstrip and stripline Reflection and terminations for logic gates, fan-out, logic switching , input impedance into a transmission-line section, reflection coefficient, skin-effect, dispersion

UNIT II
MULTI-CONDUCTOR TRANSMISSION LINES AND CROSS-TALK
Multi-conductor transmission-lines, coupling physics, per unit length parameters ,Near and far-end cross-talk, minimizing cross-talk (stripline and microstrip) Differential signalling, termination, balanced circuits ,S-parameters, Lossy and Lossles models

UNIT III
NON-IDEAL EFFECTS
Non-ideal signal return paths – gaps, BGA fields, via transitions , Parasitic inductance and capacitance , Transmission line losses – Rs, tanδ , routing parasitic, Common-mode current, differential-mode current , Connectors
UNIT IV POWER CONSIDERATIONS AND SYSTEM DESIGN 9
SSN/SSO, DC power bus design, layer stack up, SMT decoupling, Logic families, power consumption, and system power delivery, Logic families and speed Package types and parasitic, SPICE, IBIS models, Bit streams, PRBS and filtering functions of link-path components, Eye diagrams, jitter, inter-symbol interference Bit-error rate, Timing analysis

UNIT V CLOCK DISTRIBUTION AND CLOCK OSCILLATORS 9
Timing margin, Clock slew, low impedance drivers, terminations, Delay Adjustments, canceling parasitic capacitance, Clock jitter.

OUTCOMES:
- Ability to identify sources affecting the speed of digital circuits.
- Able to improve the signal transmission characteristics.

REFERENCES:

TOOLS REQUIRED
1. SPICE, source - http://www-cad.eecs.berkeley.edu/Software/software.html

AP5091 DIGITAL CONTROL ENGINEERING

OBJECTIVES:
- Students should acquire a fundamental understanding of digital control systems and design.
- To teach the fundamental concepts of Digital Control systems and mathematical modeling of the system
- To study the concept of time response and frequency response of the discrete time system
- To teach the basics of stability analysis of the digital system

UNIT I PRINCIPLES OF CONTROLLERS 9
Review of frequency and time response analysis and specifications of control systems, need for controllers, continues time compensations, continues time PI, PD, PID controllers, digital PID controllers.

UNIT II SIGNAL PROCESSING IN DIGITAL CONTROL 9
Sampling, time and frequency domain description, aliasing, hold operation, mathematical model of sample and hold, zero and first order hold, factors limiting the choice of sampling rate, reconstruction.
UNIT III  MODELING AND ANALYSIS OF SAMPLED DATA CONTROL SYSTEM  9
Difference equation description, Z-transform method of description, pulse transfer function, time and frequency response of discrete time control systems, stability of digital control systems, Jury’s stability test, state variable concepts, first companion, second companion, Jordan canonical models, discrete state variable models, elementary principles.

UNIT IV  DESIGN OF DIGITAL CONTROL ALGORITHMS  9
Review of principle of compensator design, Z-plane specifications, digital compensator design using frequency response plots, discrete integrator, discrete differentiator, development of digital PID controller, transfer function, design in the Z-plane.

UNIT V  PRACTICAL ASPECTS OF DIGITAL CONTROL ALGORITHMS  9
Algorithm development of PID control algorithms, software implementation, implementation using microprocessors and microcontrollers, finite word length effects, choice of data acquisition systems, microcontroller based temperature control systems, microcontroller based motor speed control systems.

TOTAL: 45 PERIODS

OUTCOMES:
- Acquire working knowledge of discrete system science-related mathematics.
- Design a discrete system, component or process to meet desired needs.
- Identify, formulate and solve discrete control engineering problems.
- Use the techniques, tools and skills related to discrete signals, computer science and modern discrete control engineering in modern engineering practice
- Communicate system related concepts effectively.

REFERENCES :

AP5191  EMBEDDED SYSTEM DESIGN  L T P C  3 0 0 3

OBJECTIVES :
The students should be made to:
- Learn design challenges and design methodologies
- Study general and single purpose processor
- Understand bus structures

UNIT I  EMBEDDED SYSTEM OVERVIEW  9
Embedded System Overview, Design Challenges – Optimizing Design Metrics, Design Methodology, RT-Level Combinational and Sequential Components, Optimizing Custom Single-Purpose Processors.
UNIT II  GENERAL AND SINGLE PURPOSE PROCESSOR  
Basic Architecture, Pipelining, Superscalar and VLIW architectures, Programmer’s view, Development Environment, Application-Specific Instruction-Set Processors (ASIPs) Microcontrollers, Timers, Counters and watchdog Timer, UART, LCD Controllers and Analog-to-Digital Converters, Memory Concepts.

UNIT III  BUS STRUCTURES  

UNIT IV  STATE MACHINE AND CONCURRENT PROCESS MODELS  

UNIT V  EMBEDDED SOFTWARE DEVELOPMENT TOOLS AND RTOS  

TOTAL : 45 PERIODS

OUTCOMES:
At the end of this course, the students should be able to:
- Explain different protocols
- Discuss state machine and design process models
- Outline embedded software development tools and RTOS

REFERENCES:

AP5251  SOFT COMPUTING AND OPTIMIZATION TECHNIQUES  
L  T  P  C
3  0  0  3

OBJECTIVES:
- To learn various Soft computing frameworks.
- To familiarizes with the design of various neural networks.
- To understand the concept of fuzzy logic.
- To gain insight onto Neuro Fuzzy modeling and control.
- To gain knowledge in conventional optimization techniques.
- To understand the various evolutionary optimization techniques.
UNIT I  NEURAL NETWORKS  9
Machine Learning using Neural Network, Learning algorithms, Supervised Learning Neural Networks – Feed Forward Networks, Radial Basis Function, Unsupervised Learning Neural Networks – Self Organizing map, Adaptive Resonance Architectures, Hopfield network

UNIT II  FUZZY LOGIC  9

UNIT III  NEURO-FUZZY MODELING  9

UNIT IV  CONVENTIONAL OPTIMIZATION TECHNIQUES  9

UNIT V  EVOLUTIONARY OPTIMIZATION TECHNIQUES  9
Genetic algorithm - working principle, Basic operators and Terminologies, Building block hypothesis, Travelling Salesman Problem, Particle swarm optimization, Ant colony optimization.

OUTCOMES:
Upon Completion of the course, the students will be able to
• Implement machine learning through Neural networks.
• Develop a Fuzzy expert system.
• Model Neuro Fuzzy system for clustering and classification.
• Able to use the optimization techniques to solve the real world problems

REFERENCES:
VL5006  RECONFIGURABLE ARCHITECTURES  L T P C  3 0 0 3

OBJECTIVES:
The students should be made to:
- Understand concept of reconfigurable systems
- Learn programmed FPGAs
- Study flexibility on routability

UNIT I  INTRODUCTION  9

UNIT II  FPGA TECHNOLOGIES & ARCHITECTURE  9
Technology trends- Programming technology- SRAM programmed FPGAs, antifuse programmed FPGAs, erasable programmable logic devices. Alternative FPGA architectures: Mux Vs LUT based logic blocks – CLB Vs LAB Vs Slices- Fast carry chains- Embedded RAMs- FPGA Vs ASIC design styles.

UNIT III  ROUTING FOR FPGAS  9

UNIT IV  HIGH LEVEL DESIGN  9
FPGA Design style: Technology independent optimization- technology mapping- Placement. High-level synthesis of reconfigurable hardware, high- level languages, Design tools: Simulation (cycle based, event driven based) – Synthesis (logic/HDL vs physically aware) – timing analysis (static vs dynamic)- verification physical design tools.

UNIT V  APPLICATION DEVELOPMENT WITH FPGAS  9
Case Studies of FPGA Applications–System on a Programmable Chip (SoPC) Designs.

TOTAL : 45 PERIODS

OUTCOMES:
At the end of this course, the students should be able to:
- Compare FPGA routing architectures
- Discuss FPGA applications
- Explain high level synthesis
REFERENCES:

VL5007 ADVANCED MICROPROCESSOR AND ARCHITECTURES L T P C
3 0 0 3

OBJECTIVES:
- To study 80386 and pentium processor
- To understand CISC and RISC Architectures
- To Learn ARM processor

UNIT I 80386 AND PENTIUM PROCESSOR

UNIT II CISC and RISC Architecture
Introduction to RISC architectures: RISC Versus CISC – RISC Case studies: MIPS R4000 – SPARC – Intel i860 - IBM RS/6000.

UNIT III ARM PROCESSOR

UNIT IV ARM ADDRESSING MODES AND INSTRUCTION SET

UNIT V PIC MICROCONTROLLER AND MOTOROLA 68HC11 MICROCONTROLLER

TOTAL: 45 PERIODS
OUTCOMES:
At the end of this course, the students should be able to:
- Discuss ARM addressing modes
- Outline ARM instruction set
- Explain PIC microcontroller and motorola 68HC11 microcontroller

REFERENCES:

VL5008 SELECTED TOPICS IN ASIC DESIGN

OBJECTIVES:
- The course focuses on the semi custom IC Design and introduces the principles of design logic cells, I/O cells and interconnect architecture, with equal importance given to FPGA and ASIC styles.
- The entire FPGA and ASIC design flow is dealt with from the circuit and layout design point of view.

UNIT I INTRODUCTION TO ASICS, CMOS LOGIC AND ASIC LIBRARY DESIGN
Types of ASICs - Design flow - CMOS transistors - Combinational Logic Cell – Sequential logic cell - Data path logic cell - Transistors as Resistors - Transistor Parasitic Capacitance- Logical effort.

UNIT II PROGRAMMABLE ASICS, PROGRAMMABLE ASIC LOGIC CELLS AND PROGRAMMABLE ASIC I/O CELLS
Anti fuse - static RAM - EPROM and EEPROM technology - Actel ACT - Xilinx LCA –Altera FLEX - Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks.

UNIT III PROGRAMMABLE ASIC ARCHITECTURE

UNIT IV LOGIC SYNTHESIS, PLACEMENT AND ROUTING
Logic synthesis - ASIC floor planning- placement and routing – power and clocking strategies.
UNIT V  HIGH PERFORMANCE ALGORITHMS FOR ASICS/ SOCS. SOC
CASE STUDIES  9
DAA and computation of FFT and DCT. High performance filters using delta-sigma modulators. Case
Studies: Digital camera, SDRAM, High speed data standards.

TOTAL : 45 PERIODS

OUTCOMES:
After completing this course:
• The student would have gained knowledge in the circuit design aspects at the next transistor
and block level abstractions of FPGA and ASIC design. In combination with the course on CAD
for VLSI, the student would have gained sufficient theoretical knowledge for carrying out FPGA
and ASIC designs.

REFERENCES:
2. Jose E. France, Yannis Tsividis, "Design of Analog - Digital VLSI Circuits for
5. Roger Woods, John McAllister, Dr. Ying Yi, Gaye Lightbod, “FPGA-based Implementation

VL5009  DESIGN AND ANALYSIS OF COMPUTER ALGORITHMS  L T P C
3 0 0 3

OBJECTIVES:
• To discuss the algorithmic complexity parameters and the basic algorithmic design techniques.
• To discuss the graph algorithms, algorithms for NP Completeness Approximation Algorithms
and NP Hard Problems.

UNIT I  INTRODUCTION  9
Polynomial and Exponential algorithms, big "oh" and small "oh" notation, exact algorithms and
heuristics, direct / indirect / deterministic algorithms, static and dynamic complexity, stepwise
refinement.

UNIT II  DESIGN TECHNIQUES  9
Subgoals method, working backwards, work tracking, branch and bound algorithms for traveling
salesman problem and knapsack problem, hill climbing techniques, divide and conquer method,
dynamic programming, greedy methods.

UNIT III  SEARCHING AND SORTING  9
Sequential search, binary search, block search, Fibonacci search, bubble sort, bucket sorting, quick
sort, heap sort, average case and worst case behavior

UNIT IV  GRAPH ALGORITHMS  9
Minimum spanning, tree, shortest path algorithms, R-connected graphs, Even's and Kleitman's
algorithms, max-flow min cut theorem, Steiglitz's link deficit algorithm.
UNIT V  SELECTED TOPICS  9

TOTAL: 45 PERIODS

OUTCOMES:
- Will be able to apply the suitable algorithm according to the given optimization problem.
- Ability to modify the algorithms to refine the complexity parameters.

REFERENCES:

VL5010  DEVICE MODELING – II  L T P C  3 0 0 3

OBJECTIVES:
- To understand device physics and device modelling aspects
- To study simulators to characterize the device models

UNIT I  MOSFET DEVICE PHYSICS  9
MOSFET Basic operation, Level 1, Level 2, Level 3 models, Noise sources in MOSFET, Flicker noise modeling, Thermal noise modelling, Influence of process variation, modeling of device mismatch for Analog/RF Applications

UNIT II  DEVICE MODELLING  9
Prime importance of circuit and device simulations in VLSI; Nodal, mesh, modified nodal and hybrid analysis equations. Solution of network equations: Sparse matrix techniques, solution of nonlinear networks through Newton-Raphson technique, convergence and stability.

UNIT III  MULTISTEP METHODS  9
Solution of stiff systems of equations, adaptation of multistep methods to the solution of electrical networks, general purpose circuit simulators.

UNIT IV  MATHEMATICAL TECHNIQUES FOR DEVICE SIMULATIONS  9
Poisson equation, continuity equation, drift-diffusion equation, Schrodinger equation, hydrodynamic equations, trap rate, finite difference solutions to these equations in 1D and 2D space, grid generation.

UNIT V  SIMULATION OF DEVICES  9
Computation of characteristics of simple devices like p-n junction, MOS capacitor and MOSFET; Small-signal analysis.

TOTAL : 45 PERIODS
OUTCOMES:
- To design and model MOSFET devices, taking into consideration process dependant parameters
- To utilize device level simulators

REFERENCES:

AP5292 DIGITAL IMAGE PROCESSING L T P C 3 0 0 3

OBJECTIVES:
The students should be made to:
- Understand fundamentals of digital images
- Learn different image transforms
- Study concept of segmentation

UNIT I DIGITAL IMAGE FUNDAMENTALS 9
A simple image model, Sampling and Quantization, Imaging Geometry, Digital Geometry, Image Acquisition Systems, Different types of digital images. Basic concepts of digital distances, distance transform, medial axis transform, component labeling, thinning, morphological processing, extension to gray scale morphology.

UNIT II IMAGE TRANSFORMS 9
1D DFT, 2D transforms - DFT, DCT, Discrete Sine, Walsh, Hadamard, Slant, Haar, KLT, SVD, Wavelet transform.

UNIT III SEGMENTATION OF GRAY LEVEL IMAGES 9
Histogram of gray level images, multilevel thresholding, Optimal thresholding using Bayesian classification, Watershed and Dam Construction algorithms for segmenting gray level image. Detection of edges and lines: First order and second order edge operators, multi-scale edge detection, Canny’s edge detection algorithm, Hough transform for detecting lines and curves, edge linking.

UNIT IV IMAGE ENHANCEMENT AND COLOR IMAGE PROCESSING 9
Point processing, Spatial Filtering, Frequency domain filtering, multi-spectral image enhancement, image restoration. Color Representation, Laws of color matching, chromaticity diagram, color enhancement, color image segmentation, color edge detection, color demosaicing.
UNIT V  IMAGE COMPRESSION

Lossy and lossless compression schemes, prediction based compression schemes, vector quantization, sub-band encoding schemes, JPEG compression standard, Fractal compression scheme, Wavelet compression scheme.

TOTAL : 45 PERIODS

OUTCOMES:
At the end of this course, the students should be able to:

- Discuss image enhancement techniques
- Explain color image processing
- Compare image compression schemes

REFERENCES:

VL5091  MEMS AND NEMS  L T P C

3 0 0 3

OBJECTIVES:

- To introduce the concepts of microelectromechanical devices.
- To know the fabrication process of Microsystems.
- To know the design concepts of micro sensors and micro actuators.
- To familiarize concepts of quantum mechanics and nano systems.

UNIT I  OVERVIEW


UNIT II  MEMS FABRICATION TECHNOLOGIES

UNIT III MICRO SENSORS
MEGS Sensors: Design of Acoustic wave sensors, resonant sensor, Vibratory gyroscope, Capacitive and Piezo Resistive Pressure sensors- engineering mechanics behind these Microsensors. Case study: Piezo-resistive pressure sensor.

UNIT IV MICRO ACTUATORS

UNIT V NANOSYSTEMS AND QUANTUM MECHANICS
Atomic Structures and Quantum Mechanics, Molecular and Nanostructure Dynamics: Schrodinger Equation and Wave function Theory, Density Functional Theory, Nanostructures and Molecular Dynamics, Electromagnetic Fields and their quantization, Molecular Wires and Molecular Circuits.

OUTCOMES:
At the end of this course, the student should be able to:
- Discuss micro sensors
- Explain micro actuators
- Outline nanosystems and Quantum mechanics

REFERENCES:

VL5011 SCRIPTING LANGUAGES FOR VLSI

OBJECTIVES:
The students should be made to:
- Study scripting languages
- Understand security issues
- Learn concept of TCL phenomena

UNIT I INTRODUCTION TO SCRIPTING AND PERL
Characteristics of scripting languages, Introduction to PERL, Names and values, Variables and assignment, Scalar expressions, Control structures, Built-in functions, Collections of Data, Working with arrays, Lists and hashes, Simple input and output, Strings, Patterns and regular expressions, Subroutines, Scripts with arguments.

UNIT II ADVANCED PERL
Finer points of Looping, Subroutines, Using Pack and Unpack, Working with files, Navigating the file system, Type globs, Eval, References, Data structures, Packages, Libraries and modules, Objects, Objects and modules in action, Tied variables, Interfacing to the operating systems, Security issues.
UNIT III TCL
The TCL phenomena, Philosophy, Structure, Syntax, Parser, Variables and data in TCL, Control flow, Data structures, Simple input/output, Procedures, Working with Strings, Patterns, Files and Pipes, Example code.

UNIT IV ADVANCED TCL

UNIT V TK AND JAVA SCRIPT

TOTAL : 45 PERIODS

OUTCOMES:
At the end of this course, the students should be able to:
- Explain advanced TCL
- Discuss TK and Java script

REFERENCES:
3. Guido van Rossum, and Fred L. Drake ", Python Tutorial, Jr., editor, Release 2.6.4
UNIT III HARDWARE / SOFTWARE CO-SYNTHESIS
The Co-Synthesis Problem, State-Transition Graph, Refinement and Controller Generation, Co-Synthesis Algorithm for Distributed System- Case Studies with any one application

UNIT IV PROTOTYPING AND EMULATION

UNIT V DESIGN SPECIFICATION AND VERIFICATION

TOTAL: 45 PERIODS

OUTCOMES:
• To assess prototyping and emulation techniques
• To compare hardware / software co-synthesis.
• To formulate the design specification and validate its functionality by simulation

REFERENCES:

VL5012 SELECTED TOPICS IN IC DESIGN

OBJECTIVES:
• This course deals with the supply circuit modules which are crucial modules in an IC design. Clock generation circuits play a major role in High Speed Broad Band Communication circuits, High Speed I/O’s, Memory modules and Data Conversion Circuits.
• This course focuses on the design aspect of Clock Generation circuits and their design constraints.

UNIT I VOLTAGE AND CURRENT REFERENCES
Current Mirrors, Self Biased Current Reference, startup circuits, VBE based Current Reference, VT Based Current Reference, Band Gap Reference , Supply Independent Biasing, Temperature Independent Biasing, PTAT Current Generation, Constant Gm Biasing

UNIT II LOW DROP OUT REGULATORS
UNIT III OSCILLATOR FUNDAMENTALS
General considerations, Ring oscillators, LC oscillators, Colpitts Oscillator, Jitter and Phase noise in
Ring Oscillators, Impulse Sensitivity Function for Ring Oscillators, Phase Noise in Differential LC
Oscillators.

UNIT IV PHASE LOCK LOOPS
PLL Fundamental, PLL stability, Noise Performance, Charge-Pump PLL Topology, CPPLL Building
blocks, Jitter and Phase Noise performance.

UNIT V CLOCK AND DATA RECOVERY
CDR Architectures, Tias and Limiters, CMOS Interface, Linear Half Rate CMOS CDR Circuits, Wide
capture Range CDR Circuits.

TOTAL: 45 PERIODS

OUTCOMES:
This course provides the essential know how to a designer to construct Supply reference circuits and
Clock Generation Circuits for given design specifications and aids the designer to understand the
design specifications related to Supply and Clock Generation Circuits.

REFERENCES:
2003.
3. Gabriel.A. Rincon-Mora, “Voltage references from diode to precision higher order
4. High Speed Clock and Data Recovery, High-performance Amplifiers Power Management “