ANNA UNIVERSITY, CHENNAI
AFFILIATED INSTITUTIONS
M.E. VLSI DESIGN
REGULATIONS – 2017
CHOICE BASED CREDIT SYSTEM
CURRICULA AND SYLLABI

PROGRAM OUTCOMES (POs)

Engineering Graduates will be able to:

1. **Engineering knowledge**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
2. **Problem analysis**: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
3. **Design/development of solutions**: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
4. **Conduct investigations of complex problems**: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
5. **Modern tool usage**: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
6. **The engineer and society**: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
7. **Environment and sustainability**: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
8. **Ethics**: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
9. **Individual and team work**: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
10. **Communication**: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
11. **Project management and finance**: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

12. **Life-long learning**: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

The Programme Educational Objectives (PEOs) are,

1. To equip the graduates to have an in-depth knowledge along with new technical ideas, to analyse and evaluate the potential engineering problems and to contribute to the research and development in the core areas by using modern engineering and IT tools.
2. To demonstrate self – management and teamwork in a collaborative and multidisciplinary arena
3. To inculcate good professional practices with a responsibility to contribute to sustainable development of society.
4. To have a zeal for improving technical competency by continuous and corrective learning.

The Programme Specific Objectives (PSOS) are,

1. To design and develop VLSI circuits to optimise power and area requirements, free from faults and dependencies by modelling, simulation and testing.
2. To develop VLSI systems by learning advanced algorithms, architectures and software – hardware co – design.
3. To communicate engineering concepts effectively by exhibiting high standards of technical presentations and scientific documentations.

MAPPING OF PROGRAMME EDUCATIONAL OBJECTIVES WITH PROGRAMME OUTCOMES:

A broad relation between the Programme Educational Objectives (PEO) and the Program Outcomes (PO) is given in the following table.

PROGRAMME EDUCATIONAL OBJECTIVES	PROGRAMME OUTCOMES											
	A	**B**	**C**	**D**	**E**	**F**	**G**	**H**	**I**	**J**	**K**	**L**
PEO1	1	1	1	1	1	3	3	3	2	3	3	2
PEO2	1	2	2	2	3	1	1	1	1	2	1	2
PEO3	2	2	2	2	2	3	3	3	3	1	3	1

1. Strong **2. Significant** **3. Reasonable**

SEMESTER COURSE WISE PO MAPPING

YEAR	SEMESTER	COURSE TITLE	a	b	c	d	e	f	g	h	i	j	k	l
YEAR I	SEM I	Applied Mathematics for Electronics Engineers	2	1	1	1	3	3	3	3	3	3	2	2
		Advanced Digital System Design	1	2	2	3	2	3	3	3	2	3	3	2
		CMOS Digital VLSI Design	1	2	2	2	2	3	3	3	3	3	3	3
		DSP Integrated Circuits	1	1	2	2	2	3	3	3	3	3	3	3
		CAD for VLSI Circuits	1	1	2	2	1	3	2	3	3	3	3	2
		Analog IC Design	1	1	2	2	1	3	3	3	3	3	3	3
		VLSI Design Lab I	1	1	1	1	1	3	3	3	2	2	2	2
	SEM II	Testing of VLSI Circuits	1	2	2	2	1	3	2	3	3	3	3	3
		VLSI Signal Processing	1	1	1	1	2	3	3	3	3	3	3	3
		Low Power VLSI Design	1	1	1	1	2	3	1	1	2	**3**	**1**	**2**
		Professional Elective I												
		Professional Elective II												
		Professional Elective III												
		VLSI Design Lab II	1	1	1	1	1	3	3	3	2	**2**	**2**	**2**
		Term Paper Writing and Seminar	1	3	3	2	3	3	3	3	1	**1**	**1**	2
YEAR II	SEM III	Analog to Digital Interfaces	1	2	2	2	1	3	3	3	2	3	2	3
		Professional Elective IV												
		Professional Elective V												
		Project Work Phase-I	1	1	1	1	1	3	3	3	3	**3**	**2**	**2**
	SEM IV	Project Work Phase-II	1	1	1	1	1	3	3	3	3	3	2	2

ELECTIVES														
	SEM II ELECTIVE I	Device Modeling - I	1	2	2	2	1	3	3	3	3	3	3	3
		RF IC Design	1	2	1	1	1	3	2	3	3	3	2	3
		Design of Analog Filters and Signal Conditioning Circuits	1	2	1	1	2	3	3	3	3	3	2	3
		Nano Scale Devices	1	3	3	3	2	3	3	3	3	3	3	3
	SEM II ELECTIVE II	DSP Architectures and Programming	1	2	2	3	3	3	3	3	3	3	3	3
		Networks on Chip	1	3	3	3	1	3	2	3	2	3	2	3
		Signal Integrity for High Speed Design	1	1	2	2	1	3	2	3	3	3	3	3
		Digital Control Engineering												
	SEM II ELECTIVE III	Embedded System Design	1	2	2	2	2	3	3	3	3	3	3	3
		Soft Computing and Optimization Techniques	1	1	1	1	1	3	3	3	3	3	3	3
		Reconfigurable Architectures	1	2	2	2	2	2	3	3	3	3	3	3
		Advanced Microprocessors and Architectures	1	2	2	2	2	2	3	3	3	3	3	3
	SEM III ELECTIVE IV	Selected Topics in ASIC Design	2	2	2	2	2	3	3	3	3	3	3	3
		Design and Analysis of Computer Algorithms	1	2	2	2	2	3	3	3	3	3	3	3
		Device Modeling - II	1	2	2	2	1	3	3	3	3	3	3	3
		Digital Image Processing	2	2	2	2	2	2	3	3	3	3	3	3
	SEM III ELECTIVE V	MEMS and NEMS	1	3	3	3	2	3	3	3	3	3	3	3
		Scripting Languages for VLSI	1	1	1	1	1	3	3	3	3	3	3	3
		Hardware – Software Co-design	1	1	1	1	1	3	2	3	2	3	2	3
		Selected Topics in IC Design												

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SEMESTER I

SL. NO	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C
THEORY								
1.	MA5152	Applied Mathematics for Electronics Engineers	FC	4	4	0	0	4
2.	AP5151	Advanced Digital System Design	PC	3	3	0	0	3
3.	VL5101	CMOS Digital VLSI Design	PC	3	3	0	0	3
4.	VL5191	DSP Integrated Circuits	PC	3	3	0	0	3
5.	VL5102	CAD for VLSI Circuits	PC	3	3	0	0	3
6.	VL5103	Analog IC Design	PC	4	4	0	0	4
PRACTICALS								
7.	VL5111	VLSI Design Laboratory I	PC	4	0	0	4	2
			TOTAL	**24**	**20**	**0**	**4**	**22**

SEMESTER II

SL. NO	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C
THEORY								
1.	VL5201	Testing of VLSI Circuits	PC	3	3	0	0	3
2.	VL5291	VLSI Signal Processing	PC	3	3	0	0	3
3.	VL5202	Low Power VLSI Design	PC	3	3	0	0	3
4.		Professional Elective I	PE	3	3	0	0	3
5.		Professional Elective II	PE	3	3	0	0	3
6.		Professional Elective III	PE	3	3	0	0	3
PRACTICALS								
7.	VL5211	VLSI Design Laboratory II	PC	4	0	0	4	2
8.	CP5281	Term Paper Writing and Seminar	EEC	2	0	0	2	1
			TOTAL	**24**	**18**	**0**	**6**	**21**

SEMESTER III

SL. NO	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C
THEORY								
1.	VL5301	Analog to Digital Interfaces	PC	3	3	0	0	3
2.		Professional Elective IV	PE	3	3	0	0	3
3.		Professional Elective V	PE	3	3	0	0	3
PRACTICALS								
4.	VL5311	Project Work Phase-I	EEC	12	0	0	12	6
			TOTAL	**21**	**9**	**0**	**12**	**15**

SEMESTER IV

SL. NO	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C
PRACTICALS								
1.	VL5411	Project Work Phase-II	EEC	24	0	0	24	12
			TOTAL	**24**	**0**	**0**	**24**	**12**

TOTAL NO. OF CREDITS:70

FOUNDATION COURSES (FC)

SL. NO	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C
1.	MA5152	Applied Mathematics for Electronics Engineers	FC	4	4	0	0	4

PROFESSIONAL CORE (PC)

SL. NO	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C
1.	AP5151	Advanced Digital System Design	PC	3	3	0	0	3
2.	VL5101	CMOS Digital VLSI Design	PC	3	3	0	0	3
3.	VL5191	DSP Integrated Circuits	PC	3	3	0	0	3
4.	VL5102	CAD for VLSI Circuits	PC	3	3	0	0	3
5.	VL5103	Analog IC Design	PC	4	4	0	0	4
6.	VL5111	VLSI Design Laboratory I	PC	4	0	0	4	2
7.	VL5201	Testing of VLSI Circuits	PC	3	3	0	0	3
8.	VL5291	VLSI Signal Processing	PC	3	3	0	0	3
9.	VL5202	Low Power VLSI Design	PC	3	3	0	0	3
10.	VL5211	VLSI Design Laboratory II	PC	4	0	0	4	2
11.	VL5301	Analog to Digital Interfaces	PC	3	3	0	0	3

EMPLOYABILITY ENHANCEMENT COURSE (EEC)

SL. NO	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C
1.	CP5281	Term Paper Writing and Seminar	EEC	2	0	0	2	1
2.	VL5311	Project Work Phase – I	EEC	12	0	0	12	6
3.	VL5411	Project Work Phase – II	EEC	24	0	0	24	12

PROFESSIONAL ELECTIVES (PE)*
SEMESTER II
ELECTIVE I

SL. NO	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C
1.	VL5001	Device Modeling - I	PE	3	3	0	0	3
2.	VL5002	RF IC Design	PE	3	3	0	0	3
3.	VL5003	Design of Analog Filters and Signal Conditioning Circuits	PE	3	3	0	0	3
4.	VL5004	Nano Scale Devices	PE	3	3	0	0	3

SEMESTER II
ELECTIVE II

SL. NO	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C
1.	AP5072	DSP Architectures and Programming	PE	3	3	0	0	3
2.	VL5005	Networks on Chip	PE	3	3	0	0	3
3.	AP5094	Signal Integrity for High Speed Design	PE	3	3	0	0	3
4.	AP5091	Digital Control Engineering	PE	3	3	0	0	3

SEMESTER II
ELECTIVE III

SL. NO	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C
1.	AP5191	Embedded System Design	PE	3	3	0	0	3
2.	AP5251	Soft Computing and Optimization Techniques	PE	3	3	0	0	3
3.	VL5006	Reconfigurable Architectures	PE	3	3	0	0	3
4.	VL5007	Advanced Microprocessors and Architectures	PE	3	3	0	0	3

SEMESTER III
ELECTIVE IV

SL. NO	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C
1.	VL5008	Selected Topics in ASIC Design	PE	3	3	0	0	3
2.	VL5009	Design and Analysis of Computer Algorithms	PE	3	3	0	0	3
3.	VL5010	Device Modeling- II	PE	3	3	0	0	3
4.	AP5292	Digital Image Processing	PE	3	3	0	0	3

SEMESTER III
ELECTIVE V

SL. NO	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C
1.	VL5091	MEMS and NEMS	PE	3	3	0	0	3
2.	VL5011	Scripting Languages for VLSI	PE	3	3	0	0	3
3.	AP5291	Hardware – Software Co-Design	PE	3	3	0	0	3
4.	VL5012	Selected Topics in IC Design	PE	3	3	0	0	3

MA5152 APPLIED MATHEMATICS FOR ELECTRONICS ENGINEERS **L T P C**
4 0 0 4

OBJECTIVES:

The main objective of this course is to demonstrate various analytical skills in applied mathematics and extensive experience with the tactics of problem solving and logical thinking applicable in electronics engineering. This course also will help the students to identify, formulate, abstract, and solve problems in electrical engineering using mathematical tools from a variety of mathematical areas, including fuzzy logic, matrix theory, probability, dynamic programming and queuing theory.

UNIT I FUZZY LOGIC 12

Classical logic – Multivalued logics – Fuzzy propositions – Fuzzy quantifiers.

UNIT II MATRIX THEORY 12

Cholesky decomposition - Generalized Eigenvectors - Canonical basis - QR factorization - Least squares method - Singular value decomposition.

UNIT III PROBABILITY AND RANDOM VARIABLES 12

Probability – Axioms of probability – Conditional probability – Baye's theorem - Random variables - Probability function – Moments – Moment generating functions and their properties – Binomial, Poisson, Geometric, Uniform, Exponential, Gamma and Normal distributions – Function of a Random variable.

UNIT IV DYNAMIC PROGRAMMING 12

Dynamic programming – Principle of optimality – Forward and backward recursion – Applications of dynamic programming – Problem of dimensionality.

UNIT V QUEUEING MODELS 12

Poisson Process – Markovian queues – Single and multi server models – Little's formula - Machine interference model – Steady state analysis – Self service queue.

TOTAL: 60 PERIODS

OUTCOMES:

After completing this course, students should demonstrate competency in the following skills:

- Concepts of fuzzy sets, knowledge representation using fuzzy rules, fuzzy logic, fuzzy prepositions and fuzzy quantifiers and applications of fuzzy logic.
- Apply various methods in matrix theory to solve system of linear equations.
- Computation of probability and moments, standard distributions of discrete and continuous random variables and functions of a random variable.
- Conceptualize the principle of optimality and sub-optimization, formulation and computational procedure of dynamic programming
- Exposing the basic characteristic features of a queuing system and acquire skills in analyzing queuing models.
- Using discrete time Markov chains to model computer systems.

REFERENCES:

1. Bronson, R., "Matrix Operations", Schaum's Outline Series, McGraw Hill, 2011.
2. George, J. Klir. and Yuan, B., "Fuzzy sets and Fuzzy logic, Theory and Applications", Prentice Hall of India Pvt. Ltd., 1997.
3. Gross, D., Shortle J. F., Thompson, J.M., and Harris, C. M., "Fundamentals of Queueing Theory", 4th Edition, John Wiley, 2014.
4. Johnson, R.A., Miller, I and Freund J., "Miller and Freund's Probability and Statistics for Engineers", Pearson Education, Asia, 8th Edition, 2015.
5. Taha, H.A., "Operations Research: An Introduction", 9th Edition, Pearson Education, Asia, New Delhi, 2016.

AP5151 ADVANCED DIGITAL SYSTEM DESIGN L T P C
3 0 0 3

OBJECTIVES:

- To introduce methods to analyze and design synchronous and asynchronous sequential circuits
- To introduce the architectures of programmable devices
- To introduce design and implementation of digital circuits using programming tools

UNIT I SEQUENTIAL CIRCUIT DESIGN 9

Analysis of clocked synchronous sequential circuits and modeling- State diagram, state table, state table assignment and reduction-Design of synchronous sequential circuits design of iterative circuits-ASM chart and realization using ASM

UNIT II ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN 9

Analysis of asynchronous sequential circuit – flow table reduction-races-state assignment-transition table and problems in transition table- design of asynchronous sequential circuit-Static, dynamic and essential hazards – data synchronizers – mixed operating mode asynchronous circuits – designing vending machine controller

UNIT III FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS 9

Fault table method-path sensitization method – Boolean difference method-D algorithm - Tolerance techniques – The compact algorithm – Fault in PLA – Test generation-DFT schemes – Built in self test

UNIT IV SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES 9

Programming logic device families – Designing a synchronous sequential circuit using PLA/PAL – Realization of finite state machine using PLD – FPGA – Xilinx FPGA-Xilinx 4000

UNIT V SYSTEM DESIGN USING VERILOG 9

Hardware Modelling with Verilog HDL – Logic System, Data Types and Operators For Modelling in Verilog HDL - Behavioural Descriptions in Verilog HDL – HDL Based Synthesis – Synthesis of Finite State Machines– structural modeling – compilation and simulation of Verilog code –Test bench - Realization of combinational and sequential circuits using Verilog – Registers – counters – sequential machine – serial adder – Multiplier- Divider – Design of simple microprocessor

TOTAL : 45 PERIODS

OUTCOMES:

At the end of the course, the student should be able to:

- Analyze and design sequential digital circuits
- Identify the requirements and specifications of the system required for a given application
- Design and use programming tools for implementing digital circuits of industry standards

REFERENCES:

1. Charles H.Roth Jr “Fundamentals of Logic Design” Thomson Learning 2004
2. M.D.Ciletti , Modeling, Synthesis and Rapid Prototyping with the Verilog HDL, Prentice Hall, 1999
3. M.G.Arnold, Verilog Digital – Computer Design, Prentice Hall (PTR), 1999.
4. Nripendra N Biswas “Logic Design Theory” Prentice Hall of India,2001
5. Parag K.Lala “Fault Tolerant and Fault Testable Hardware Design” B S
6. Publications,2002
7. Parag K.Lala “Digital system Design using PLD” B S Publications,2003
8. S. Palnitkar , Verilog HDL – A Guide to Digital Design and Synthesis, Pearson , 2003.

VL5101 **CMOS DIGITAL VLSI DESIGN** **L T P C**
3 0 0 3

OBJECTIVES:

- This course deals comprehensively with all aspects of transistor level design of all the digital building blocks common to all CMOS microprocessors, DPSs, network processors, digital backend of all wireless systems etc.
- The focus will be on the transistor level design and will address all important issues related to size, speed and power consumption. The units are classified according to the important building and will introduce the principles and design methodology in terms of the dominant circuit choices, constraints and performance measures.

UNIT I MOS TRANSISTOR PRINCIPLES AND CMOS INVERTER 12

MOS(FET) Transistor Characteristic under Static and Dynamic Conditions, MOS Transistor Secondary Effects, Process Variations, Technology Scaling, Internet Parameter and electrical wise models CMOS Inverter - Static Characteristic, Dynamic Characteristic, Power, Energy, and Energy Delay parameters.

UNIT II COMBINATIONAL LOGIC CIRCUITS 9

Propagation Delays, Stick diagram, Layout diagrams, Examples of combinational logic design, Elmore's constant, Dynamic Logic Gates, Pass Transistor Logic, Power Dissipation, Low Power Design principles.

UNIT III SEQUENTIAL LOGIC CIRCUITS 9

Static Latches and Registers, Dynamic Latches and Registers, Timing Issues, Pipelines, Pulse and sense amplifier based Registers, Nonbistable Sequential Circuits.

UNIT IV ARITHMETIC BUILDING BLOCKS AND MEMORY ARCHITECTURES 9

Data path circuits, Architectures for Adders, Accumulators, Multipliers, Barrel Shifters, Speed and Area Tradeoffs, Memory Architectures, and Memory control circuits.

UNIT V INTERCONNECT AND CLOCKING STRATEGIES 6

Interconnect Parameters – Capacitance, Resistance, and Inductance, Electrical Wire Models, Timing classification of Digital Systems, Synchronous Design, Self-Timed Circuit Design.

TOTAL: 45 PERIODS

OUTCOMES:

At the end of the course, the student should be able to:

- Carry out transistor level design of the most important building blocks used in digital CMOS VLSI circuits.
- Discuss design methodology of arithmetic building block
- Analyze tradeoffs of the various circuit choices for each of the building block.

REFERENCES:

1. Jan Rabaey, Anantha Chandrakasan, B Nikolic, "Digital Integrated Circuits: A Design Perspective". Second Edition, Feb 2003, Prentice Hall of India.
2. Jacob Baker "CMOS: Circuit Design, Layout, and Simulation, Third Edition", Wiley IEEE Press 2010 3rd Edition.
3. M J Smith, "Application Specific Integrated Circuits", Addisson Wesley, 1997
4. N.Weste, K. Eshraghian, " Principles of CMOS VLSI Design". Second Edition, 1993 Addision Wesley.

VL5191 DSP INTEGRATED CIRCUITS L T P C
3 0 0 3

OBJECTIVES:

- To familiarize the concept of DSP and DSP algorithms.
- Introduction to Multirate systems and finite wordlength effects
- To know about the basic DSP processor architectures and the synthesis of the processing elements

UNIT I INTRODUCTION TO DSP INTEGRATED CIRCUITS 9

Introduction to Digital signal processing, Sampling of analog signals, Selection of sample frequency, Signal- processing systems, Frequency response, Transfer functions, Signal flow graphs, Filter structures, Adaptive DSP algorithms, DFT-The Discrete Fourier Transform, FFT Algorithm, Image coding, Discrete cosine transforms, Standard digital signal processors, Application specific ICs for DSP, DSP systems, DSP system design, Integrated circuit design.

UNIT II DIGITAL FILTERS AND FINITE WORD LENGTH EFFECTS 9

FIR filters, FIR filter structures, FIR chips, IIR filters, Specifications of IIR filters, Mapping of analog transfer functions, Mapping of analog filter structures, Multi rate systems, Interpolation with an integer factor L, Sampling rate change with a ratio L/M, Multi rate filters. Finite word length effects - Parasitic oscillations, Scaling of signal levels, Round-off noise, Measuring round-off noise, Coefficient sensitivity, Sensitivity and noise.

UNIT III DSP ARCHITECTURES 9

DSP system architectures, Standard DSP architecture-Harvard and Modified Harvard architecture. Ideal DSP architectures, Multiprocessors and multi computers, Systolic and Wave front arrays, Shared memory architectures.

UNIT IV SYNTHESIS OF DSP ARCHITECTURES 9

Synthesis: Mapping of DSP algorithms onto hardware, Implementation based on complex PEs, Shared memory architecture with Bit – serial PEs. Combinational & sequential networks- Storage elements – clocking of synchronous systems, Asynchronous systems -FSM

UNIT V ARITHMETIC UNIT AND PROCESSING ELEMENTS 9

Conventional number system, Redundant Number system, Residue Number System, Bit-parallel and Bit-Serial arithmetic, Digit Serial arithmetic, CORDIC Algorithm, Basic shift accumulator, Reducing the memory size, Complex multipliers, Improved shift-accumulator. Case Study: DCT and FFT processor

TOTAL: 45 PERIODS

OUTCOMES:

- Get to know about the Digital Signal Processing concepts and its algorithms
- Get an idea about finite word length effects in digital filters
- Concept behind multi rate systems is understood.
- Get familiar with the DSP processor architectures and how to perform synthesis of processing elements

REFERENCES:

1. B.Venkatramani, M.Bhaskar, “Digital Signal Processors”, Tata McGraw-Hill, 2002.
2. John J. Proakis, Dimitris G. Manolakis, “Digital Signal Processing”, Pearson Education, 2002.
3. Keshab Parhi, “VLSI Digital Signal Processing Systems design & Implementation”, John Wiley & Sons, 1999.
4. Lars Wanhammer, “DSP Integrated Circuits”, Academic press, New York, 1999.

VL5102 CAD FOR VLSI CIRCUITS L T P C
3 0 0 3

OBJECTIVES:
The students should be made to:
- Learn VLSI Design methodologies
- Understand VLSI design automation tools
- Study modelling and simulation

UNIT I INTRODUCTION TO VLSI DESIGN FLOW 9
Introduction to VLSI Design methodologies, Basics of VLSI design automation tools, Algorithmic Graph Theory and Computational Complexity, Tractable and Intractable problems, General purpose methods for combinatorial optimization.

UNIT II LAYOUT, PLACEMENT AND PARTITIONING 9
Layout Compaction, Design rules, Problem formulation, Algorithms for constraint graph compaction, Placement and partitioning, Circuit representation, Placement algorithms, Partitioning

UNIT III FLOOR PLANNING AND ROUTING 9
Floor planning concepts, Shape functions and floorplan sizing, Types of local routing problems, Area routing, Channel routing, Global routing, Algorithms for global routing.

UNIT IV SIMULATION AND LOGIC SYNTHESIS 9
Simulation, Gate-level modeling and simulation, Switch-level modeling and simulation, Combinational Logic Synthesis, Binary Decision Diagrams, Two Level Logic Synthesis.

UNIT V HIGH LEVEL SYNTHESIS 9
Hardware models for high level synthesis, internal representation, allocation, assignment and scheduling, scheduling algorithms, Assignment problem, High level transformations.

TOTAL: 45 PERIODS

OUTCOMES:
At the end of this course, the students should be able to:
- Outline floor planning and routing
- Explain Simulation and Logic Synthesis
- Discuss the hardware models for high level synthesis

REFERENCES:

1. N.A. Sherwani, "Algorithms for VLSI Physical Design Automation", Kluwer Academic Publishers, 2002.
2. S.H. Gerez, "Algorithms for VLSI Design Automation", John Wiley & Sons, 2002.
3. Sadiq M. Sait, Habib Youssef, “VLSI Physical Design automation: Theory and Practice”, World Scientific 1999.
4. Steven M.Rubin, “Computer Aids for VLSI Design”, Addison Wesley Publishing 1987.

VL5103 **ANALOG IC DESIGN** **L T P C**
4 0 0 4

OBJECTIVES

- To study MOS devices modelling and scaling effects.
- To familiarize the design of single stage and multistage MOS amplifier and analysis their frequency responses.
- To study the different design parameters in designing voltage reference and OPAMP circuits.

UNIT I MOSFET METRICS 12

Simple long channel MOSFET theory – SPICE Models – Technology trend, Need for Analog design - Sub-micron transistor theory, Short channel effects, Narrow width effect, Drain induced barrier lowering, Sub-threshold conduction, Reliability, Digital metrics, Analog metrics, Small signal parameters, Unity Gain Frequency, Miller's approximation

UNIT II SINGLE STAGE AND TWO STAGE AMPLIFIERS 12

Single Stage Amplifiers – Common source amplifier with resistive load, diode load, constant current load, Source degeneration Source follower, Input and output impedance, Common gate amplifier - Differential Amplifiers – differential and common mode response, Input swing, gain, diode load and constant current load - Basic Two Stage Amplifier, Cut-off frequency, poles and zeros

UNIT III FREQUENCY RESPONSE OF SINGLE STAGE AND TWO STAGE AMPLIFIERS 12

Frequency Response of Single Stage Amplifiers – Noise in Single stage Amplifiers – Stability and Frequency Compensation in Single stage Amplifiers, Frequency Response of Two Stage Amplifiers, – Noise in two stage Amplifiers – Stability, gain and phase margins, Frequency Compensation in two stage Amplifiers, Effect of loading in feedback networks,

UNIT IV CURRENT MIRRORS AND REFERENCE CIRCUITS 12

Cascode, Negative feedback, Wilson, Regulated cascode, Bandgap voltage reference, Constant Gm biasing, supply and temperature independent reference, curvature compensation, trimming, Effect of transistor mismatch in analog design

UNIT V OP AMPS 12

Gilbert cell and applications, Basic two stage OPAMP, two-pole system response, common mode and differential gain, Frequency response of OPAMP, CMFB circuits, slew rate, power supply rejection ratio, random offset, systematic offset, Noise, Output stage, OTA and OPAMP circuits - Low voltage OPAMP

TOTAL : 60 PERIODS

OUTCOMES:

- To design MOS single stage, multistage amplifiers and OPAMP for desired frequencies
- Analyze Stability, frequency response, and Noise in MOS amplifiers

REFERENCES:

1. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", McGraw Hill, 2000
2. Philip E.Allen, "CMOS Analog Circuit Design", Oxford University Press, 2013
3. Paul R.Gray, "Analysis and Design of Analog Integrated Circuits", Wiley Student edition, 5th edition, 2009.
4. R.Jacob Baker, "CMOS: Circuit Design, Layout , and Simulation", Wiley Student Edition, 2009

VL5111 **VLSI DESIGN LABORATORY I** **L T P C**
0 0 4 2

OBJECTIVES:

The laboratory based study for the entire program is clubbed under three categories. One is the FPGA based design methodology; the second is the simulation of analog building blocks, and analog and digital CAD design flow. Experiments pertaining to the former two topics are covered in this lab course and those pertaining to the latter will be covered in VLSI Design Lab II.

FPGAs are important platform used throughout the industry both in their own right in building complete systems. They are also used as validation/verification platforms prior to undertaking cost and time intensive design and fabrication of custom VLSI designs. Starting from high level design entry in the form VHDL/Verilog codes, the students will be carrying out complete hardware level FPGA validation of important digital algorithms. In addition, exercises on the SPICE simulation of the basic CMOS analog building blocks will be carried out.

EXPERIMENTS:

1. Understanding Synthesis principles. Back annotation.
2. Test vector generation and timing analysis of sequential and combinational logic design realized using HDL languages.
3. FPGA real time programming and I/O interfacing.
4. Interfacing with Memory modules in FPGA Boards.
5. Verification of design functionality implemented in FPGA by capturing the signal in DSO.
6. Real time application development.
7. Design Entry Using VHDL or Verilog examples for Digital circuit descriptions using HDL languages sequential, concurrent statements and structural description.

TOTAL : 60 PERIODS

OUTCOMES:

At the end of the course, the student should be able to: After completing this course, given a digital system specification, the student should be able to map it onto FPGA paltform and carry out a series of validations design starting from design entry to hardware testing. In addition, the student also will be able to design and carry out time domain and frequency domain simulations of simple analog building blocks, study the pole zero behaviors of feedback based circuits and compute the input/output impedances.

VL5201 **TESTING OF VLSI CIRCUITS** **L T P C**
3 0 0 3

OBJECTIVES :

The students should be made to:

- Understand logic fault models
- Learn test generation for sequential and combinational logic circuits

UNIT I TESTING AND FAULT MODELLING 9

Introduction to testing – Faults in Digital Circuits – Modelling of faults – Logical Fault Models –Fault detection – Fault Location – Fault dominance – Logic simulation – Types of simulation –Delay models – Gate Level Event – driven simulation.

UNIT II TEST GENERATION 9

Test generation for combinational logic circuits – Testable combinational logic circuit design – Test generation for sequential circuits – design of testable sequential circuits.

UNIT III DESIGN FOR TESTABILITY 9

Design for Testability – Ad-hoc design – generic scan based design – classical scan based design– system level DFT approaches.

UNIT IV SELF – TEST AND TEST ALGORITHMS 9

Built-In self-test – test pattern generation for BIST – Circular BIST – BIST Architectures – Testable Memory Design – Test Algorithms – Test generation for Embedded RAMs.

UNIT V FAULT DIAGNOSIS 9

Logical Level Diagnosis – Diagnosis by UUT reduction – Fault Diagnosis for Combinational Circuits– Self-checking design – System Level Diagnosis.

TOTAL : 45 PERIODS

OUTCOMES:

At the end of this course, the students should be able to:

- Prepare design for testability
- Discuss test algorithms
- Explain fault diagnosis

REFERENCES:

1. A.L.Crouch, "Design Test for Digital IC's and Embedded Core Systems", Prentice HallInternational, 2002.
2. M.Abramovici, M.A.Breuer and A.D. Friedman, "Digital systems and Testable Design", JaicoPublishing House, 2002.
3. M.L.Bushnell and V.D.Agrawal, "Essentials of Electronic Testing for Digital, Memory andMixed-
   Signal VLSI Circuits", Kluwer Academic Publishers, 2002.
4. P.K. Lala, "Digital Circuit Testing and Testability", Academic Press, 2002.

VL5291	VLSI SIGNAL PROCESSING	L T P C
		3 0 0 3

OBJECTIVES:

- To introduce techniques for altering the existing DSP structures to suit VLSI implementations.
- To introduce efficient design of DSP architectures suitable for VLSI

UNIT I PIPELINING AND PARALLEL PROCESSING OF DIGITAL FILTERS 9

Introduction to DSP systems – Typical DSP algorithms, Data flow and Dependence graphs – critical path, Loop bound, iteration bound, Longest path matrix algorithm, Pipelining and Parallel processing of FIR filters, Pipelining and Parallel processing for low power.

UNIT II ALGORITHMIC STRENGTH REDUCTION TECHNIQUE I 9

Retiming – definitions and properties, Unfolding – an algorithm for unfolding, properties of unfolding, sample period reduction and parallel processing application, Algorithmic strength reduction in filters and transforms – 2-parallel FIR filter, 2-parallel fast FIR filter, DCT architecture, rank-order filters, Odd-Even merge-sort architecture, parallel rank-order filters.

UNIT III ALGORITHIMIC STRENGTH REDUCTION -II 9

Fast convolution – Cook-Toom algorithm, modified Cook-Toom algorithm, Pipelined and parallel recursive filters – Look-Ahead pipelining in first-order IIR filters, Look-Ahead pipelining with powerof-2 decomposition, Clustered look-ahead pipelining, Parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters.

UNIT IV BIT-LEVEL ARITHMETIC ARCHITECTURES 9

Bit-level arithmetic architectures – parallel multipliers with sign extension, parallel carry-ripple and carry-save multipliers, Design of Lyon‟s bit-serial multipliers using Horner‟s rule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner‟s rule for precision improvement, Distributed Arithmetic fundamentals and FIR filters

UNIT V NUMERICAL STRENGTH REDUCTION, WAVE AND ASYNCHRONOUS PIPELINING 9

Numerical strength reduction – subexpression elimination, multiple constant multiplication, iterative matching, synchronous pipelining and clocking styles, clock skew in edge-triggered single phase clocking, two-phase clocking, wave pipelining. Asynchronous pipelining bundled data versus dual rail protocol.

TOTAL: 45 PERIODS

OUTCOME:

- Ability to modify the existing or new DSP architectures suitable for VLSI.

REFERENCES:

1. Keshab K. Parhi, " VLSI Digital Signal Processing Systems, Design and implementation ", Wiley, Interscience, 2007.
2. U. Meyer – Baese, " Digital Signal Processing with Field Programmable Gate Arrays", Springer, Second Edition, 2004.

VL5202 LOW POWER VLSI DESIGN L T P C
3 0 0 3

OBJECTIVES:

- Identify sources of power in an IC.
- Identify the power reduction techniques based on technology independent and technology dependent
- Power dissipation mechanism in various MOS logic style.
- Identify suitable techniques to reduce the power dissipation.
- Design memory circuits with low power dissipation.

UNIT I POWER DISSIPATION IN CMOS 9

Physics of power dissipation in CMOS FET devices – Hierarchy of limits of power – Sources of power consumption – Static Power Dissipation, Active Power Dissipation - Designing for Low Power, Circuit Techniques For Leakage Power Reduction - Basic principle of low power design.

UNIT II POWER OPTIMIZATION 9

Logic level power optimization – Circuit level low power design – Standard Adder Cells, CMOS Adders Architectures-BiCMOS adders - Low Voltage Low Power Design Techniques, Current Mode Adders -Types Of Multiplier Architectures, Braun, Booth and Wallace Tree Multipliers and their performance comparison

UNIT III DESIGN OF LOW POWER CMOS CIRCUITS 9

Computer arithmetic techniques for low power system – low voltage low power static Random access and dynamic Random access memories – low power clock, Inter connect and layout design – Advanced techniques – Special techniques.

UNIT IV POWER ESTIMATION 9

Power Estimation techniques – logic power estimation – Simulation power analysis –Probabilistic power analysis.

UNIT V SYNTHESIS AND SOFTWARE DESIGN FOR LOW POWER 9

Synthesis for low power – Behavioral level transform – software design for low power.

TOTAL: 45 PERIODS

OUTCOMES:

- The student will get to know the basics and advanced techniques in low power design which is a hot topic in today‟s market where the power plays major role.
- The reduction in power dissipation by an IC earns a lot including reduction in size, cost and etc.

REFERENCES:

1. AbdelatifBelaouar, Mohamed.I.Elmasry, "Low power digital VLSI design", Kluwer, 1995.
2. A.P.Chandrasekaran and R.W.Broadersen, "Low power digital CMOS design", Kluwer,1995.
3. DimitriosSoudris, C.Pignet, Costas Goutis,"Designing CMOS Circuits for Low Power"Kluwer, 2002.
4. Gary Yeap, "Practical low power digital VLSI design", Kluwer, 1998.
5. James B.Kulo, Shih-Chia Lin, "Low voltage SOI CMOS VLSI devices and Circuits", John Wiley and sons, inc. 2001.
6. J.B.Kulo and J.H Lou, "Low voltage CMOS VLSI Circuits", Wiley 1999.
7. Kaushik Roy and S.C.Prasad, "Low power CMOS VLSI circuit design", Wiley, 2000.
8. Kiat-send Yeo, Kaushik Roy "Low-Voltage, Low-power VLSI Subsystem", Tata McGraw-Hill, 2009

VL5211 VLSI DESIGN LABORATORY II L T P C
0 0 4 2

OBJECTIVE:

The focus of this course the CAD based VLSI design flow. The entire VLSI design industry makes use of this design flow in some for or the other. Proficiency and familiarity with the various stages of a typical 'state of this design flow is a prerequisite for any student who wishes to be apart of either the industry or their search in VLSI over one full semester exposure to various stages of a typical state of the art CAD VLSI tool be provided by various experiments designed to bring out the key aspects of simulation, and power and clock routing modules. ASIC RTL realization of an available open source MCU

EXPERIMENTS :

To synthesize and understand the Boolean optimization in synthesis. Static timing analyses procedures and constraints. Critical path considerations. Scan chain insertion, Floor planning, Routing and Placement procedures. Power planning, Layout generation, LVS and back annotation, Total power estimate. Analog circuit simulation. Simulation of logic gates, Current mirrors, Current sources, Differential amplifier in Spice.
Layout generations, LVS, Back annotation

TOTAL: 60 PERIODS

OUTCOMES:

The student would have hands on experience in the carrying out a complete VLSI based experiments using / CADENCE/ TANNER/ Mentor/Synopsis

CP5281 **TERM PAPER WRITING AND SEMINAR** **L T P C**
0 0 2 1

In this course, students will develop their scientific and technical reading and writing skills that they need to understand and construct research articles. A term paper requires a student to obtain information from a variety of sources (i.e., Journals, dictionaries, reference books) and then place it in logically developed ideas. The work involves the following steps:

1. Selecting a subject, narrowing the subject into a topic
2. Stating an objective.
3. Collecting the relevant bibliography (atleast 15 journal papers)
4. Preparing a working outline.
5. Studying the papers and understanding the authors contributions and critically analysing each paper.
6. Preparing a working outline
7. Linking the papers and preparing a draft of the paper.
8. Preparing conclusions based on the reading of all the papers.
9. Writing the Final Paper and giving final Presentation

Please keep a file where the work carried out by you is maintained.
Activities to be carried Out

Activity	**Instructions**	**Submission week**	**Evaluation**
Selection of area of interest and Topic Stating an Objective	You are requested to select an area of interest, topic and state an objective	2nd week	**3 %** Based on clarity of thought, current relevance and clarity in writing
Collecting Information about your area & topic	1. List 1 Special Interest Groups or professional society 2. List 2 journals 3. List 2 conferences, symposia or workshops 4. List 1 thesis title 5. List 3 web presences (mailing lists, forums, news sites) 6. List 3 authors who publish regularly in your area 7. Attach a call for papers (CFP) from your area.	3rd week	**3%** (the selected information must be area specific and of international and national standard)
Collection of Journal papers in the topic in the context of the objective – collect 20 & then filter	• You have to provide a complete list of references you will be using- Based on your objective -Search various digital libraries and Google Scholar • When picking papers to read - try to: • Pick papers that are related to each other in some ways and/or that are in the same field so that you can write a meaningful survey out of them, • Favour papers from well-known journals and conferences,	4th week	**6%** (the list of standard papers and reason for selection)

	• Favour "first" or "foundational" papers in the field (as indicated in other people's survey paper), • Favour more recent papers, • Pick a recent survey of the field so you can quickly gain an overview, • Find relationships with respect to each other and to your topic area (classification scheme/categorization) • Mark in the hard copy of papers whether complete work or section/sections of the paper are being considered		
Reading and notes for first 5 papers	Reading Paper Process • For each paper form a Table answering the following questions: • What is the main topic of the article? • What was/were the main issue(s) the author said they want to discuss? • Why did the author claim it was important? • How does the work build on other's work, in the author's opinion? • What simplifying assumptions does the author claim to be making? • What did the author do? • How did the author claim they were going to evaluate their work and compare it to others? • What did the author say were the limitations of their research? • What did the author say were the important directions for future research? Conclude with limitations/issues not addressed by the paper (from the perspective of your survey)	5th week	**8%** (the table given should indicate your understanding of the paper and the evaluation is based on your conclusions about each paper)
Reading and notes for next5 papers	Repeat Reading Paper Process	6th week	**8%** (the table given should indicate your understanding of the paper and the evaluation is based on your conclusions about each paper)
Reading and notes for final 5 papers	Repeat Reading Paper Process	7th week	**8%** (the table given should indicate your understanding of the paper and the evaluation is based on your conclusions about each paper)

Draft outline 1 and Linking papers	Prepare a draft Outline, your survey goals, along with a classification / categorization diagram	8th week	**8%** (this component will be evaluated based on the linking and classification among the papers)
Abstract	Prepare a draft abstract and give a presentation	9th week	**6%** (Clarity, purpose and conclusion) **6%** Presentation & Viva Voce
Introduction Background	Write an introduction and background sections	10th week	**5%** (clarity)
Sections of the paper	Write the sections of your paper based on the classification / categorization diagram in keeping with the goals of your survey	11thweek	**10%** (this component will be evaluated based on the linking and classification among the papers)
Your conclusions	Write your conclusions and future work	12th week	**5%** (conclusions – clarity and your ideas)
Final Draft	Complete the final draft of your paper	13th week	**10%** (formatting, English, Clarity and linking) **4%** Plagiarism Check Report
Seminar	A brief 15 slides on your paper	14th & 15th week	**10%** (based on presentation and Viva-voce)

TOTAL : 30 PERIODS

VL5301 ANALOG TO DIGITAL INTERFACES L T P C
3 0 0 3

OBJECTIVES

- To understand the importance of sampling the input analog signal for digitization and enabling circuit architectures
- To understand the principles of Analog to Digital and Digital to Analog conversion of signals.
- To understand the importance of calibration techniques for achieving precision during data conversion

UNIT I SAMPLE AND HOLD CIRCUITS 9

Sampling switches, Conventional open loop and closed loop sample and hold architecture, Open loop architecture with miller compensation, multiplexed input architectures, recycling architecture switched capacitor architecture.

UNIT II SWITCHED CAPACITOR CIRCUITS AND COMPARATORS 9

Switched-capacitor amplifiers, switched capacitor integrator, switched capacitor common mode feedback. Single stage amplifier as comparator, cascaded amplifier stages as comparator, latched comparators.

UNIT III DIGITAL TO ANALOG CONVERSION 9

Performance metrics, reference multiplication and division, switching and logic functions in DAC, Resistor ladder DAC architecture, current steering DAC architecture.

UNIT IV ANALOG TO DIGITAL CONVERSION 9

Performance metric, Flash architecture, Pipelined Architecture, Successive approximation architecture, Time interleaved architecture.

UNIT V PRECISION TECHNIQUES 9

Comparator offset cancellation, Op Amp offset cancellation, Calibration techniques, range overlap and digital correction.

TOTAL: 45 PERIODS

OUTCOMES:

- To be able to design Analog to Digital and Digital to Analog data converters based on data precision requirements

REFERENCE:

1. Behzad Razavi, "Principles of data conversion system design", S. Chand and company Ltd, 2000.

VL5001 DEVICE MODELING - I L T P C
3 0 0 3

OBJECTIVES

- To study the MOS capacitors and to model MOS Transistors
- To understand the various CMOS design parameters and their impact on performance of the device.
- To study the device level characteristics of BJT transistors

UNIT I MOS CAPACITORS 9

Surface Potential: Accumulation, Depletion, and Inversion, Electrostatic Potential and Charge Distribution in Silicon, Capacitances in an MOS Structure, Polysilicon-Gate Work Function and Depletion Effects, MOS under Nonequilibrium and Gated Diodes, Charge in Silicon Dioxide and at the Silicon–Oxide Interface, Effect of Interface Traps and Oxide Charge on Device Characteristics, High-Field Effects, Impact Ionization and Avalanche Breakdown, Band-to-Band Tunneling, Tunneling into and through Silicon Dioxide, Injection of Hot Carriers from Silicon into Silicon Dioxide, High-Field Effects in Gated Diodes, Dielectric Breakdown

UNIT II MOSFET DEVICES 9

Long-Channel MOSFETs, Drain-Current Model, MOSFET I–V Characteristics, Subthreshold Characteristics, Substrate Bias and Temperature Dependence of Threshold Voltage, MOSFET Channel Mobility, MOSFET Capacitances and Inversion-Layer Capacitance Effect, Short-Channel MOSFETs, Short-Channel Effect, Velocity Saturation and High-Field Transport Channel Length Modulation, Source–Drain Series Resistance, MOSFET Degradation and Breakdown at High Fields

UNIT III CMOS DEVICE DESIGN 9

MOSFET Scaling, Constant-Field Scaling, Generalized Scaling, Nonscaling Effects, Threshold Voltage, Threshold-Voltage Requirement, Channel Profile Design, Nonuniform Doping, Quantum Effect on Threshold Voltage, Discrete Dopant Effects on Threshold Voltage, MOSFET Channel Length, Various Definitions of Channel Length, Extraction of the Effective Channel Length, Physical Meaning of Effective Channel Length, Extraction of Channel Length by C–V Measurements

UNIT IV CMOS PERFORMANCE FACTORS 9

Basic CMOS Circuit Elements, CMOS Inverters, CMOS NAND and NOR Gates, Inverter and NAND Layouts, Parasitic Elements, Source–Drain Resistance, Parasitic Capacitances, Gate Resistance, Interconnect R and C, Sensitivity of CMOS Delay to Device Parameters, Propagation Delay and Delay Equation, Delay Sensitivity to Channel Width, Length, and Gate Oxide Thickness, Sensitivity of Delay to Power-Supply Voltage and Threshold Voltage, Sensitivity of Delay to Parasitic Resistance and Capacitance, Delay of Two-Way NAND and Body Effect, Performance Factors of Advanced CMOS Devices, MOSFETs in RF Circuits, Effect of Transport Parameters on CMOS Performance, Low-Temperature CMOS

UNIT V BIPOLAR DEVICES 9

n–p–n Transistors, Basic Operation of a Bipolar Transistor, Modifying the Simple Diode Theory for Describing Bipolar Transistors, Ideal Current–Voltage Characteristics, Collector Current, Base Current, Current Gains, Ideal IC–VCE Characteristics, Characteristics of a Typical n–p–n Transistor, Effect of Emitter and Base Series Resistances, Effect of Base–Collector Voltage on Collector Current, Collector Current Falloff at High Currents, Nonideal Base Current at Low Currents, Bipolar Device Models for Circuit and Time-Dependent Analyses Basic dc Model, Basic ac Model, Small-Signal Equivalent-Circuit Model, Emitter Diffusion Capacitance, Charge-Control Analysis, Breakdown Voltages, Common-Base Current Gain in the Presence of Base–Collector Junction Avalanche, Saturation Currents in a Transistor, Relation Between BV_{CEO} and BV_{CBO}.

TOTAL: 45 PERIODS

OUTCOMES:

To design and model MOSFET and BJT devices to desired specifications.

REFERENCES:

1. Behzad Razavi, “Fundamentals of Microelectronics” Wiley Student Edition, 2nd Edition.
2. J P Collinge, C A Collinge, “Physics of Semiconductor devices” Springer 2002 Edition.
3. Yuan Taur and Tak H. Ning, "Fundamentals of Modern VLSI Devices", Cambridge University Press, Second Edition.

VL5002 RF IC DESIGN L T P C
3 0 0 3

OBJECTIVES:

- To study the various impedance matching techniques used in RF circuit design.
- To understand the functional design aspects of LNAs, Mixers, PLLs and VCO.
- To understand frequency synthesis.

UNIT I IMPEDANCE MATCHING IN AMPLIFIERS 9

Definition of ‘Q’, series parallel transformations of lossy circuits, impedance matching using ‘L’, ‘PI’ and T networks, Integrated inductors, resistors, Capacitors, tunable inductors, transformers

UNIT II AMPLIFIER DESIGN **9**

Noise characteristics of MOS devices, Design of CG LNA and inductor degenerated LNAs. Principles of RF Power Amplifiers design,

UNIT III ACTIVE AND PASSIVE MIXERS **9**

Qualitative Description of the Gilbert Mixer - Conversion Gain, and distortion and noise , analysis of Gilbert Mixer – Switching Mixer - Distortion in Unbalanced Switching Mixer -Conversion Gain in Unbalanced Switching Mixer - Noise in Unbalanced Switching Mixer - A Practical Unbalanced Switching Mixer. Sampling Mixer - Conversion Gain in Single Ended Sampling Mixer - Distortion in Single Ended Sampling Mixer - Intrinsic Noise in Single Ended Sampling Mixer - Extrinsic Noise in Single Ended Sampling Mixer.

UNIT IV OSCILLATORS **9**

LC Oscillators, Voltage Controlled Oscillators, Ring oscillators, Delay Cells, tuning range in ring oscillators, Tuning in LC oscillators, Tuning sensitivity, Phase Noise in oscillators, sources of phase noise

UNIT V PLL AND FREQUENCY SYNTHESIZERS **9**

Phase Detector/Charge Pump, Analog Phase Detectors, Digital Phase Detectors, Frequency Dividers, Loop Filter Design, Phase Locked Loops, Phase noise in PLL, Loop Bandwidth, Basic Integer-N frequency synthesizer, Basic Fractional-N frequency synthesizer

TOTAL: 45 PERIODS

OUTCOMES:

To understand the principles of operation of an RF receiver front end and be able to design and apply constraints for LNAs, Mixers and Frequency synthesizers

REFERENCES:

1. B.Razavi ,"RF Microelectronics" , Prentice-Hall ,1998
2. Bosco H Leung "VLSI for Wireless Communication", Pearson Education, 2002
3. Behzad Razavi, "Design of Analog CMOS Integrated Circuits" McGraw-Hill, 1999
4. Jia-sheng Hong, "Microstrip filters for RF/Microwave applications", Wiley, 2001
5. Thomas H.Lee, "The Design of CMOS Radio –Frequency Integrated Circuits', Cambridge University Press ,2003

VL5003 DESIGN OF ANALOG FILTERS AND SIGNAL CONDITIONING CIRCUITS **L T P C 3 0 0 3**

OBJECTIVE:

This course deals with CMOS circuit design of various Analog Filter architectures. The required signal conditioning techniques in a Mixed signal IC environment are also dealt in this course.

UNIT I FILTER TOPOLOGIES **9**

The Bilinear Transfer Function - Active RC Implementation, Transconductor-C Implementation, Switched Capacitor Implementation, Biquadratic Transfer Function, Active RC implementation, Switched capacitor implementation, High Q, Q peaking and instability, Transconductor-C Implementation, the Digital Biquad.

UNIT II INTEGRATOR REALIZATION **9**

Lowpass Filters, Active RC Integrators – Effect of finite Op-Amp Gain Bandwidth Product, Active RC SNR, gm-C Integrators, Discrete Time Integrators.

UNIT III SWITCHED CAPACITOR FILTER REALIZATION 9

Switched capacitor Technique, Biquadratic SC Filters, SC N-path filters, Finite gain and bandwidth effects, Layout consideration, Noise in SC Filters.

UNIT IV SIGNAL CONDITIONING TECHNIQUES 9

Interference types and reduction, Signal circuit grounding, Shield grounding, Signal conditioners for capacitive sensors, Noise and Drift in Resistors, Layout Techniques.

UNIT V SIGNAL CONDITIONING CIRCUITS 9

Isolation Amplifiers, Chopper and Low Drift Amplifiers, Electrometer and Transimpedance Amplifiers, Charge Amplifiers, Noise in Amplifiers

TOTAL : 45 PERIODS

OUTCOMES:

The student will apply the operational and design principles for all the important active analog filter configurations. The student also will gain working knowledge of signal conditioning techniques and the necessary guide lines in a Mixed signal IC environment.

REFERENCES:

1. Ramson Pallas-Areny, John G. Webster "Sensors and Signal Conditioning" , A wiley Inter science Publication, John Wiley & Sons INC,2001.
2. R.Jacob Baker, "CMOS Mixed-Signal Circuit Design", John Wiley & Sons, 2008.
3. Schauman, Xiao and Van Valkenburg, "Design of Analog Filters", Oxford University Press, 2009.

VL5004	NANO SCALE DEVICES	L T P C
		3 0 0 3

OBJECTIVES

- To introduce novel MOSFET devices and understand the advantages of multi-gate devices
- To introduce the concepts of nanoscale MOS transistor and their performance characteristics
- To study the various nano scaled MOS transistors

UNIT I INTRODUCTION TO NOVEL MOSFETS 9

MOSFET scaling, short channel effects - channel engineering - source/drain engineering - high k dielectric - copper interconnects - strain engineering, SOI MOSFET, multigate transistors – single gate – double gate – triple gate – surround gate, quantum effects – volume inversion – mobility – threshold voltage – inter subband scattering, multigate technology – mobility – gate stack

UNIT II PHYSICS OF MULTIGATE MOS SYSTEMS 9

MOS Electrostatics – 1D – 2D MOS Electrostatics, MOSFET Current-Voltage Characteristics – CMOS Technology – Ultimate limits, double gate MOS system – gate voltage effect - semiconductor thickness effect – asymmetry effect – oxide thickness effect – electron tunnel current – two dimensional confinement, scattering – mobility

UNIT III NANOWIRE FETS AND TRANSISTORS AT THE MOLECULAR SCALE 9

Silicon nanowire MOSFETs – Evaluvation of I-V characteristics – The I-V characteristics for non-degenerate carrier statistics – The I-V characteristics for degenerate carrier statistics – Carbon nanotube – Band structure of carbon nanotube – Band structure of graphene – Physical structure of nanotube – Band structure of nanotube – Carbon nanotube FETs – Carbon nanotube MOSFETs – Schottky barrier carbon nanotube FETs – Electronic conduction in molecules – General model for ballistic nano transistors – MOSFETs with 0D, 1D, and 2D channels – Molecular transistors – Single electron charging – Single electron transistors

UNIT IV RADIATION EFFECTS 9

Radiation effects in SOI MOSFETs, total ionizing dose effects – single gate SOI – multigate devices, single event effect, scaling effects

UNIT V CIRCUIT DESIGN USING MULTIGATE DEVICES 9

Digital circuits – impact of device performance on digital circuits – leakage performance trade off – multi VT devices and circuits – SRAM design, analog circuit design – transconductance - intrinsic gain – flicker noise – self heating –band gap voltage reference – operational amplifier – comparator designs, mixed signal – successive approximation DAC, RF circuits.

TOTAL : 45 PERIODS

OUTCOMES

- To design circuits using nano scaled MOS transistors with the physical insight of their functional characteristics

REFERENCES:

1. J P Colinge, "FINFETs and other multi-gate transistors", Springer – Series on integrated circuits and systems, 2008
2. Mark Lundstrom, Jing Guo, "Nanoscale Transistors: Device Physics, Modeling and Simulation", Springer, 2006
3. M S Lundstorm, "Fundamentals of Carrier Transport", 2nd Ed., Cambridge University Press, Cambridge UK, 2000

AP5072	DSP PROCESSOR ARCHITECTURE AND PROGRAMMING	L	T	P	C
		3	0	0	3

OBJECTIVES:

The objective of this course is to provide in-depth knowledge on

- Digital Signal Processor basics
- Third generation DSP Architecture and programming skills
- Advanced DSP architectures and some applications.

UNIT I FUNDAMENTALS OF PROGRAMMABLE DSPs 9

Multiplier and Multiplier accumulator – Modified Bus Structures and Memory access in PDSPs – Multiple access memory – Multi-port memory – VLIW architecture- Pipelining – Special Addressing modes in P-DSPs – On chip Peripherals.

UNIT II SPECIAL FUNCTIONS 9

Architecture – Assembly language syntax - Addressing modes – Assembly language Instructions - Pipeline structure, Operation – Block Diagram of DSP starter kit – Application Programs for processing real time signals.

UNIT III LINEAR PROGRAMMING 9

Architecture of the C6x Processor - Instruction Set - DSP Development System: Introduction – DSP Starter Kit Support Tools- Code Composer Studio - Support Files - Programming Examples to Test the DSK Tools – Application Programs for processing real time signals.

UNIT IV ALGEBRAIC EQUATIONS 9

Architecture of ADSP-21XX and ADSP-210XX series of DSP processors- Addressing modes and assembly language instructions – Application programs –Filter design, FFT calculation.

UNIT V ORDINARY DIFFERENTIAL EQUATIONS 9

Architecture of TMS320C54X: Pipe line operation, Code Composer studio – Architecture of TMS320C6X - Architecture of Motorola DSP563XX – Comparison of the features of DSP family processors.

TOTAL : 45 PERIODS

OUTCOMES:

Students should be able to:

- Become Digital Signal Processor specialized engineer
- DSP based System Developer

REFERENCES:

1. Avtar Singh and S. Srinivasan, Digital Signal Processing – Implementations using DSP Microprocessors with Examples from TMS320C54xx, cengage Learning India Private Limited, Delhi 2012
2. B.Venkataramani and M.Bhaskar, “Digital Signal Processors – Architecture, Programming and Applications” – Tata McGraw – Hill Publishing Company Limited. New Delhi, 2003.
3. RulphChassaing, Digital Signal Processing and Applications with the C6713 and C6416 DSK, A John Wiley & Sons, Inc., Publication, 2005
4. User guides Texas Instrumentation, Analog Devices, Motorola.

VL5005 NETWORKS ON CHIP L T P C
3 0 0 3

OBJECTIVES:

The students should be made to:

- Understand the concept of network - on - chip
- Learn router architecture designs
- Study fault tolerance network - on - chip

UNIT I INTRODUCTION TO NOC 9

Introduction to NoC – OSI layer rules in NoC - Interconnection Networks in Network-on-ChipNetwork Topologies - Switching Techniques - Routing Strategies - Flow Control Protocol Quality-of-Service Support

UNIT II ARCHITECTURE DESIGN 9

Switching Techniques and Packet Format - Asynchronous FIFO Design -GALS Style of Communication - Wormhole Router Architecture Design - VC Router Architecture Design - Adaptive Router Architecture Design.

UNIT III ROUTING ALGORITHM 9

Packet routing-Qos, congestion control and flow control – router design – network link design – Efficient and Deadlock-Free Tree-Based Multicast Routing Methods - Path-Based Multicast Routing for 2D and 3D Mesh Networks- Fault-Tolerant Routing Algorithms - Reliable and Adaptive Routing Algorithms

UNIT IV TEST AND FAULT TOLERANCE OF NOC 9

Design-Security in Networks-on-Chips-Formal Verification of Communications in Networks-on Chips-Test and Fault Tolerance for Networks-on-Chip Infrastructures-Monitoring Services for Networks-on-Chips.

UNIT V THREE-DIMENSIONAL INTEGRATION OF NETWORK-ON-CHIP 9

Three-Dimensional Networks-on-Chips Architectures. – A Novel Dimensionally-Decomposed Router for On-Chip Communication in 3D Architectures - Resource Allocation for QoS On-Chip Communication – Networks-on-Chip Protocols-On-Chip Processor Traffic Modeling for Networks-on-Chip

TOTAL: 45 PERIODS

OUTCOMES:

At the end of this course, the students should be able to:

- Compare different architecture design
- Discuss different routing algorithms
- Explain three dimensional networks - on-chip architectures

REFERENCES:

1. ChrysostomosNicopoulos, Vijaykrishnan Narayanan, Chita R.Das" Networks-on - Chip " Architectures Holistic Design Exploration", Springer.
2. Fayezgebali, Haythamelmiligi, HqhahedWatheq E1-Kharashi "Networks-on-Chips theory and practice CRC press.
3. Konstantinos Tatas and Kostas Siozios "Designing 2D and 3D Network-on-Chip Architectures" 2013
4. Palesi, Maurizio, Daneshtalab, Masoud "Routing Algorithms in Networks-on-Chip" 2014
5. SantanuKundu, SantanuChattopadhyay "Network-on-Chip: The Next Generation of System on-Chip Integration",2014 CRC Press

AP5094 SIGNAL INTEGRITY FOR HIGH SPEED DESIGN L T P C
3 0 0 3

OBJECTIVES:

- To identify sources affecting the speed of digital circuits.
- To introduce methods to improve the signal transmission characteristics

UNIT I SIGNAL PROPAGATION ON TRANSMISSION LINES 9

Transmission line equations, wave solution, wave *vs*. circuits, initial wave, delay time, Characteristic impedance , wave propagation, reflection, and bounce diagrams Reactive terminations – L, C , static field maps of micro strip and strip line cross-sections, per unit length parameters, PCB layer stackups and layer/Cu thicknesses, cross-sectional analysis tools, Zo and Td equations for microstrip and stripline Reflection and terminations for logic gates, fan-out, logic switching , input impedance into a transmission-line section, reflection coefficient, skin-effect, dispersion

UNIT II MULTI-CONDUCTOR TRANSMISSION LINES AND CROSS-TALK 9

Multi-conductor transmission-lines, coupling physics, per unit length parameters ,Near and far-end cross-talk, minimizing cross-talk (stripline and microstrip) Differential signalling, termination, balanced circuits ,S-parameters, Lossy and Lossles models

UNIT III NON-IDEAL EFFECTS 9

Non-ideal signal return paths – gaps, BGA fields, via transitions , Parasitic inductance and capacitance , Transmission line losses – Rs, tanδ , routing parasitic, Common-mode current, differential-mode current , Connectors

UNIT IV POWER CONSIDERATIONS AND SYSTEM DESIGN 9

SSN/SSO , DC power bus design , layer stack up, SMT decoupling ,, Logic families, power consumption, and system power delivery , Logic families and speed Package types and parasitic ,SPICE, IBIS models ,Bit streams, PRBS and filtering functions of link-path components , Eye diagrams , jitter , inter-symbol interference Bit-error rate ,Timing analysis

UNIT V CLOCK DISTRIBUTION AND CLOCK OSCILLATORS 9

Timing margin, Clock slew, low impedance drivers, terminations, Delay Adjustments, canceling parasitic capacitance, Clock jitter.

TOTAL: 45 PERIODS

OUTCOMES:

- Ability to identify sources affecting the speed of digital circuits.
- Able to improve the signal transmission characteristics.

REFERENCES:

1. Douglas Brooks, Signal Integrity Issues and Printed Circuit Board Design, Prentice Hall PTR, 2003.
2. Eric Bogatin , Signal Integrity – Simplified , Prentice Hall PTR, 2003.
3. H. W. Johnson and M. Graham, High-Speed Digital Design: A Handbook of Black Magic, Prentice Hall, 1993.
4. S. Hall, G. Hall, and J. McCall, High-Speed Digital System Design: A Handbook of Interconnect Theory and Design Practices, Wiley-Interscience, 2000.

TOOLS REQUIRED

1. SPICE, source - http://www-cad.eecs.berkeley.edu/Software/software.html
2. HSPICE from synopsis, www.synopsys.com/products/ mixedsignal/hspice/hspice.html
3. SPECCTRAQUEST from Cadence, http://www.specctraquest.com

AP5091 DIGITAL CONTROL ENGINEERING L T P C
3 0 0 3

OBJECTIVES:

- Students should acquire a fundamental understanding of digital control systems and design.
- To teach the fundamental concepts of Digital Control systems and mathematical modeling of the system
- To study the concept of time response and frequency response of the discrete time system
- To teach the basics of stability analysis of the digital system

UNIT I PRINCIPLES OF CONTROLLERS 9

Review of frequency and time response analysis and specifications of control systems, need for controllers, continues time compensations, continues time PI, PD, PID controllers, digital PID controllers.

UNIT II SIGNAL PROCESSING IN DIGITAL CONTROL 9

Sampling, time and frequency domain description, aliasing, hold operation, mathematical model of sample and hold, zero and first order hold, factors limiting the choice of sampling rate, reconstruction.

UNIT III MODELING AND ANALYSIS OF SAMPLED DATA CONTROL SYSTEM 9

Difference equation description, Z-transform method of description, pulse transfer function, time and frequency response of discrete time control systems, stability of digital control systems, Jury's stability test, state variable concepts, first companion, second companion, Jordan canonical models, discrete state variable models, elementary principles.

UNIT IV DESIGN OF DIGITAL CONTROL ALGORITHMS 9

Review of principle of compensator design, Z-plane specifications, digital compensator design using frequency response plots, discrete integrator, discrete differentiator, development of digital PID controller, transfer function, design in the Z-plane.

UNIT V PRACTICAL ASPECTS OF DIGITAL CONTROL ALGORITHMS 9

Algorithm development of PID control algorithms, software implementation, implementation using microprocessors and microcontrollers, finite word length effects, choice of data acquisition systems, microcontroller based temperature control systems, microcontroller based motor speed control systems.

TOTAL: 45 PERIODS

OUTCOMES:

- Acquire working knowledge of discrete system science-related mathematics.
- Design a discrete system, component or process to meet desired needs.
- Identify, formulate and solve discrete control engineering problems.
- Use the techniques, tools and skills related to discrete signals, computer science and modern discrete control engineering in modern engineering practice
- Communicate system related concepts effectively.

REFERENCES :

1. John J. D'Azzo, "Constantive Houpios, Linear Control System Analysis and Design", Mc Graw Hill, 1995.
2. Kenneth J. Ayala, "The 8051 Microcontroller- Architecture, Programming and Applications", Penram International, 2nd Edition, 1996.
3. M. Gopal, "Digital Control and Static Variable Methods", Tata McGraw Hill, New Delhi, 1997.

AP5191 EMBEDDED SYSTEM DESIGN L T P C

3 0 0 3

OBJECTIVES :

The students should be made to:

- Learn design challenges and design methodologies
- Study general and single purpose processor
- Understand bus structures

UNIT I EMBEDDED SYSTEM OVERVIEW 9

Embedded System Overview, Design Challenges – Optimizing Design Metrics, Design Methodology, RT-Level Combinational and Sequential Components, Optimizing Custom Single-Purpose Processors.

UNIT II GENERAL AND SINGLE PURPOSE PROCESSOR 9

Basic Architecture, Pipelining, Superscalar and VLIW architectures, Programmer's view, Development Environment, Application-Specific Instruction-Set Processors (ASIPs) Microcontrollers, Timers, Counters and watchdog Timer, UART, LCD Controllers and Analog-to-Digital Converters, Memory Concepts.

UNIT III BUS STRUCTURES 9

Basic Protocol Concepts, Microprocessor Interfacing – I/O Addressing, Port and Bus-Based I/O, Arbitration, Serial Protocols, I^2C, CAN and USB, Parallel Protocols – PCI and ARM Bus, Wireless Protocols – IrDA, Bluetooth, IEEE 802.11.

UNIT IV STATE MACHINE AND CONCURRENT PROCESS MODELS 9

Basic State Machine Model, Finite-State Machine with Datapath Model, Capturing State Machine in Sequential Programming Language, Program-State Machine Model, Concurrent Process Model, Communication among Processes, Synchronization among processes, Dataflow Model, Real-time Systems, Automation: Synthesis, Verification : Hardware/Software Co-Simulation, Reuse: Intellectual Property Cores, Design Process Models.

UNIT V EMBEDDED SOFTWARE DEVELOPMENT TOOLS AND RTOS 9

Compilation Process – Libraries – Porting kernels – C extensions for embedded systems – emulation and debugging techniques – RTOS – System design using RTOS.

TOTAL : 45 PERIODS

OUTCOMES:

At the end of this course, the students should be able to:

- Explain different protocols
- Discuss state machine and design process models
- Outline embedded software development tools and RTOS

REFERENCES:

1. Bruce Powel Douglas, "Real time UML, second edition: Developing efficient objects for embedded systems", 3rd Edition 1999, Pearson Education.
2. Daniel W. Lewis, "Fundamentals of embedded software where C and assembly meet", Pearson Education, 2002.
3. Frank Vahid and Tony Gwargie, "Embedded System Design", John Wiley & sons, 2002.
4. Steve Heath, "Embedded System Design", Elsevier, Second Edition, 2004.

AP5251	SOFT COMPUTING AND OPTIMIZATION TECHNIQUES	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To learn various Soft computing frameworks.
- To familiarizes with the design of various neural networks.
- To understand the concept of fuzzy logic.
- To gain insight onto Neuro Fuzzy modeling and control.
- To gain knowledge in conventional optimization techniques.
- To understand the various evolutionary optimization techniques

UNIT I NEURAL NETWORKS 9

Machine Learning using Neural Network, Learning algorithms, Supervised Learning Neural Networks – Feed Forward Networks, Radial Basis Function, Unsupervised Learning Neural Networks – Self Organizing map , Adaptive Resonance Architectures, Hopfield network

UNIT II FUZZY LOGIC 9

Fuzzy Sets – Operations on Fuzzy Sets – Fuzzy Relations – Membership Functions-Fuzzy Rules and Fuzzy Reasoning – Fuzzy Inference Systems – Fuzzy Expert Systems – Fuzzy Decision Making

UNIT III NEURO-FUZZY MODELING 9

Adaptive Neuro-Fuzzy Inference Systems – Coactive Neuro-Fuzzy Modeling – Classification and Regression Trees – Data Clustering Algorithms – Rule base Structure Identification –Neuro-Fuzzy Control – Case Studies.

UNIT IV CONVENTIONAL OPTIMIZATION TECHNIQUES 9

Introduction to optimization techniques, Statement of an optimization problem, classification, Unconstrained optimization-gradient search method-Gradient of a function, steepest gradient-conjugate gradient, Newton's Method, Marquardt Method, Constrained optimization –sequential linear programming, Interior penalty function method, external penalty function method.

UNIT V EVOLUTIONARY OPTIMIZATION TECHNIQUES 9

Genetic algorithm - working principle, Basic operators and Terminologies, Building block hypothesis, Travelling Salesman Problem, Particle swam optimization, Ant colony optimization.

TOTAL :45 PERIODS

OUTCOMES:

Upon Completion of the course, the students will be able to

- Implement machine learning through Neural networks.
- Develop a Fuzzy expert system.
- Model Neuro Fuzzy system for clustering and classification.
- Able to use the optimization techniques to solve the real world problems

REFERENCES:

1. David E. Goldberg, Genetic Algorithms in Search, Optimization and Machine Learning, Addison wesley, 2009.
2. George J. Klir and Bo Yuan, Fuzzy Sets and Fuzzy Logic-Theory and Applications,Prentice Hall, 1995.
3. James A. Freeman and David M. Skapura, Neural Networks Algorithms, Applications, and Programming Techniques, Pearson Edn., 2003.
4. Jyh-Shing Roger Jang, Chuen-Tsai Sun, Eiji Mizutani, Neuro-Fuzzy and Soft Computing, Prentice-Hall of India, 2003.
5. Mitchell Melanie, An Introduction to Genetic Algorithm, Prentice Hall, 1998
6. Simon Haykins, Neural Networks: A Comprehensive Foundation, Prentice Hall International Inc, 1999.
7. Singiresu S. Rao, Engineering optimization Theory and practice, John Wiley & sons, inc,Fourth Edition, 2009
8. Timothy J.Ross, Fuzzy Logic with Engineering Applications, McGraw-Hill, 1997.
9. Venkata Rao, Vimal J. Savsani, Mechanical Design Optimization Using Advanced Optimization Techniques, springer 2012

VL5006 RECONFIGURABLE ARCHITECTURES **L T P C**
3 0 0 3

OBJECTIVES :

The students should be made to:

- Understand concept of reconfigurable systems
- Learn programmed FPGAs
- Study flexibility on routability

UNIT I INTRODUCTION 9

Domain-specific processors, Application specific processors, Reconfigurable Computing Systems – Evolution of reconfigurable systems – Characteristics of RCS advantages and issues. Fundamental concepts & Design steps –classification of reconfigurable architecture-fine, coarse grain & hybrid architectures – Examples

UNIT II FPGA TECHNOLOGIES & ARCHITECTURE 9

Technology trends- Programming technology- SRAM programmed FPGAs, antifuse programmed FPGAs, erasable programmable logic devices. Alternative FPGA architectures: Mux Vs LUT based logic blocks – CLB Vs LAB Vs Slices- Fast carry chains- Embedded RAMs- FPGA Vs ASIC design styles.

UNIT III ROUTING FOR FPGAS 9

General Strategy for routing in FPGAs- routing for row-based FPGAs – segmented channel routing, definitions- Algorithm for I segment and K segment routing – Routing for symmetrical FPGAs, Flexibility of FPGA Routing Architectures: FPGA architectural flexibility on Routability- Effect of switch block flexibility on routability - Tradeoffs in flexibility of S and C blocks

UNIT IV HIGH LEVEL DESIGN 9

FPGA Design style: Technology independent optimization- technology mapping- Placement. High-level synthesis of reconfigurable hardware, high- level languages, Design tools: Simulation (cycle based, event driven based) – Synthesis (logic/HDL vs physically aware) – timing analysis (static vs dynamic)- verification physical design tools.

UNIT V APPLICATION DEVELOPMENT WITH FPGAS 9

Case Studies of FPGA Applications–System on a Programmable Chip (SoPC) Designs.

TOTAL : 45 PERIODS

OUTCOMES:

At the end of this course, the students should be able to:

- Compare FPGA routing architectures
- Discuss FPGA applications
- Explain high level synthesis

REFERENCES:

1. Christophe Bobda, “Introduction to Reconfigurable Computing –Architectures, Algorithms and Applications”, Springer, 2010.
2. Clive “Max” Maxfield, “The Design Warrior’s Guide to FPGAs: Devices, Tools And Flows”, Newnes, Elsevier, 2006.
3. Jorgen Staunstrup, Wayne Wlf, “Hardware/Software Co- Design: Priciples and practice”, Kluwer Academic Pub, 1997.
4. Maya B. Gokhale and Paul S. Graham, “Reconfigurable Computing: Accelerating Computation with Field-Programmable Gate Arrays”, Springer, 2005.
5. Russell tessier and Wayne Burleson “Reconfigurable Computing for Digital Signal Processing: A Survey” Journal of VLSI Signal processing 28,p7-27,2001.
6. Stephen M. Trimberger, “field – programmable Gate Array Technology” Springer,2007.
7. Stephen D. broen, Robert J. Francis, Jonathan Rose, Zvonko G. Vranesic,” Fieldprogrammable Gate Arrays”, Kluwer Academic Pubnlishers, 1992.
8. Scott Hauck and Andre Dehon (Eds.), “Reconfigurable Computing –The Theory and Practice of FPGA-Based Computation”, Elsevier / Morgan Kaufmann, 2008.

VL5007 ADVANCED MICROPROCESSOR AND ARCHITECTURES L T P C
3 0 0 3

OBJECTIVES:

- To study 80386 and pentium processor
- To understand CISC and RISC Architectures
- To Learn ARM processor

UNIT I 80386 AND PENTIUM PROCESSOR 9

80386 PROCESSOR: Basic programming model – Memory organization – Data types – Instruction set - Addressing mode – Address translation – Interrupts –PENTIUM PROCESSOR : Introduction to Pentium processor architecture – Special Pentium Registers – Pentium Memory Management – Introduction to Pentium pro processor – Pentium Pro Special Features.

UNIT II CISC and RISC Architecture 9

Introduction to RISC architectures: RISC Versus CISC – RISC Case studies: MIPS R4000 – SPARC – Intel i860 - IBM RS/6000.

UNIT III ARM PROCESSOR 9

ARM Programmer’s Model – Registers – Processor Modes – State of the processor – Condition Flags – ARM Pipelines – Exception Vector Table – ARM Processor Families – Typical 3 stage pipelined ARM organization–Introduction to ARM Memory Management Unit.

UNIT IV ARM ADDRESSING MODES AND INSTRUCTION SET 9

ARM Addressing Modes – ARM Instruction Set Overview – Thumb Instruction Set Overview – LPC210X ARM Processor Features.

UNIT V PIC MICROCONTROLLER AND MOTOROLA 68HC11 MICROCONTROLLER 9

Instruction set, addressing modes – operating modes- Interrupt system- RTC-Serial Communication Interface – A/D Converter PWM and UART. **MOTOROLA:** CPU Architecture – Instruction set – interrupts- Timers- I^2C Interfacing –UART- A/D Converter – PWM

TOTAL: 45 PERIODS

OUTCOMES:
At the end of this course, the students should be able to:

- Discuss ARM addressing modes
- Outline ARM instruction set
- Explain PIC microcontroller and motorola 68HC11 microcontroller

REFERENCES :

1. Andrew Sloss, "ARM System Developer's Guide", Morgan Kaufmann Publishers, 2005
2. Barry B Brey, "The Intel Microprocessor, Pentium and Pentium Pro Processor, Architecture Programming and Interfacing", Prentice Hall of India, 2002.
3. Daniel Tabak, "Advanced Microprocessors", McGraw Hill Inc., 1995.
4. David E Simon "An Embedded Software Primer", Pearson Education, 2007
5. Gene .H.Miller ." Micro Computer Engineering ," Pearson Education , 2003.
6. Intel, "Microprocessors, Vol-I & Vol-II", Intel Corporation, USA, 1992.
7. John .B.Peatman , " Design with PIC Microcontroller , Prentice hall, 1997
8. Mohammed Rafiquzzaman, "Microprocessors and Microcomputer Based System Design", Universal Book Stall, New Delhi, 1990.
9. Steve Furber, "ARM System-on-Chip Architecture", Pearson Education, 2005
   "ARM7 TDMI Technical Reference Manual", ARM Ltd., UK, 2004 6.

VL5008	**SELECTED TOPICS IN ASIC DESIGN**	**L T P C**
		3 0 0 3

OBJECTIVES:

- The course focuses on the semi custom IC Design and introduces the principles of design logic cells, I/O cells and interconnect architecture, with equal importance given to FPGA and ASIC styles.
- The entire FPGA and ASIC design flow is dealt with from the circuit and layout design point of view.

UNIT I INTRODUCTION TO ASICS, CMOS LOGIC AND ASIC LIBRARY DESIGN 9

Types of ASICs - Design flow - CMOS transistors - Combinational Logic Cell – Sequential logic cell - Data path logic cell - Transistors as Resistors - Transistor Parasitic Capacitance- Logical effort.

UNIT II PROGRAMMABLE ASICS, PROGRAMMABLE ASIC LOGIC CELLS AND PROGRAMMABLE ASIC I/O CELLS 9

Anti fuse - static RAM - EPROM and EEPROM technology - Actel ACT - Xilinx LCA –Altera FLEX - Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks.

UNIT III PROGRAMMABLE ASIC ARCHITECUTRE 9

Architecture and configuration of Spartan / Cyclone and Virtex / Stratix FPGAs – Micro-Blaze / Nios based embedded systems – Signal probing techniques.

UNIT IV LOGIC SYNTHESIS, PLACEMENT AND ROUTING 9

Logic synthesis - ASIC floor planning- placement and routing – power and clocking strategies.

UNIT V HIGH PERFORMANCE ALGORITHMS FOR ASICS/ SOCS. SOC CASE STUDIES 9

DAA and computation of FFT and DCT. High performance filters using delta-sigma modulators. Case Studies: Digital camera, SDRAM, High speed data standards.

TOTAL : 45 PERIODS

OUTCOMES:

After completing this course:

- The student would have gained knowledge in the circuit design aspects at the next transistor and block level abstractions of FPGA and ASIC design. In combination with the course on CAD for VLSI, the student would have gained sufficient theoretical knowledge for carrying out FPGA and ASIC designs.

REFERENCES:

1. Douglas J. Smith, HDL Chip Design, Madison, AL, USA: Doone Publications, 1996.
2. Jose E. France, YannisTsividis, "Design of Analog - Digital VLSI Circuits for Telecommunication and Signal Processing", Prentice Hall, 1994.
3. M.J.S.Smith, " Application - Specific Integrated Circuits", Pearson,2003
4. Mohammed Ismail and Terri Fiez, "Analog VLSI Signal and Information Processing ", McGraw Hill, 1994.
5. Roger Woods, John McAllister, Dr. Ying Yi, Gaye Lightbod, “FPGA-based Implementation of Signal Processing Systems”, Wiley, 2008
6. Steve Kilts, “Advanced FPGA Design,” Wiley Inter-Science.

VL5009	DESIGN AND ANALYSIS OF COMPUTER ALGORITHMS	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To discuss the algorithmic complexity parameters and the basic algorithmic design techniques.
- To discuss the graph algorithms, algorithms for NP Completeness Approximation Algorithms and NP Hard Problems.

UNIT I INTRODUCTION 9

Polynomial and Exponential algorithms, big "oh" and small "oh" notation, exact algorithms and heuristics, direct / indirect / deterministic algorithms, static and dynamic complexity, stepwise refinement.

UNIT II DESIGN TECHNIQUES 9

Subgoals method, working backwards, work tracking, branch and bound algorithms for traveling salesman problem and knapsack problem, hill climbing techniques, divide and conquer method, dynamic programming, greedy methods.

UNIT III SEARCHING AND SORTING 9

Sequential search, binary search, block search, Fibonacci search, bubble sort, bucket sorting, quick sort, heap sort, average case and worst case behavior

UNIT IV GRAPH ALGORITHMS 9

Minimum spanning, tree, shortest path algorithms, R-connected graphs, Even's and Kleitman's algorithms, max-flow min cut theorem, Steiglitz's link deficit algorithm.

UNIT V SELECTED TOPICS 9

NP Completeness Approximation Algorithms, NP Hard Problems, Strasseu's Matrix Multiplication Algorithms, Magic Squares, Introduction To Parallel Algorithms and Genetic Algorithms, Monte-Carlo Methods, Amortised Analysis.

TOTAL: 45 PERIODS

OUTCOMES:

- Will be able to apply the suitable algorithm according to the given optimization problem.
- Ability to modify the algorithms to refine the complexity parameters.

REFERENCES:

1. D.E.Goldberg, "Genetic Algorithms : Search Optimization and Machine Learning", Addison Wesley, 1989.
2. E.Horowitz and S.Sahni, "Fundamentals of Computer Algorithms", Galgotia Publications, 1988.
3. Sara Baase, "Computer Algorithms : Introduction to Design and Analysis", Addison Wesley, 1988.
4. T.H.Cormen, C.E.Leiserson and R.L.Rivest, "Introduction to Algorithms", Mc Graw Hill, 1994.

VL5010 DEVICE MODELING – II L T P C
3 0 0 3

OBJECTIVES:

- To understand device physics and device modelling aspects
- To study simulators to characterize the device models

UNIT I MOSFET DEVICE PHYSICS 9

MOSFET Basic operation, Level 1, Level 2, Level 3 models, Noise sources in MOSFET, Flicker noise modeling, Thermal noise modelling, Influence of process variation, modeling of device mismatch for Analog/RF Applications

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UNIT II DEVICE MODELLING 9

Prime importance of circuit and device simulations in VLSI; Nodal, mesh, modified nodal and hybrid analysis equations. **Solution of network equations:** Sparse matrix techniques, solution of nonlinear networks through Newton-Raphson technique, convergence and stability.

UNIT III MULTISTEP METHODS 9

Solution of stiff systems of equations, adaptation of multistep methods to the solution of electrical networks, general purpose circuit simulators.

UNIT IV MATHEMATICAL TECHNIQUES FOR DEVICE SIMULATIONS 9

Poisson equation, continuity equation, drift-diffusion equation, Schrodinger equation, hydrodynamic equations, trap rate, finite difference solutions to these equations in 1D and 2D space, grid generation.

UNIT V SIMULATION OF DEVICES 9

Computation of characteristics of simple devices like p-n junction, MOS capacitor and MOSFET; Small-signal analysis.

TOTAL : 45 PERIODS

OUTCOMES:

- To design and model MOSFET devices, taking into consideration process dependant parameters
- To utilize device level simulators

REFERENCES :

1. Arora, N., “MOSFET Models for VLSI Circuit Simulation”, Springer-Verlag, 1993
2. Chua, L.O. and Lin, P.M., “Computer-Aided Analysis of Electronic Circuits: Algorithms and Computational Techniques”, Prentice-Hall., 1975
3. Fjeldly, T., Yetterdal, T. and Shur, M., “Introduction to Device Modeling and Circuit Simulation”, Wiley-Interscience., 1997
4. Grasser, T., “Advanced Device Modeling and Simulation”, World Scientific Publishing Company., 2003
5. Selberherr, S., “Analysis and Simulation of Semiconductor Devices”, Springer-Verlag., 1984
6. Trond Ytterdal, Yuhua Cheng and Tor A. FjeldlyWayne Wolf, “Device Modeling for Analog and RF CMOS Circuit Design”, John Wiley & Sons Ltd.

AP5292 DIGITAL IMAGE PROCESSING L T P C
3 0 0 3

OBJECTIVES :
The students should be made to:

- Understand fundamentals of digital images
- Learn different image transforms
- Study concept of segmentation

UNIT I DIGITAL IMAGE FUNDAMENTALS 9

A simple image model, Sampling and Quantization, Imaging Geometry, Digital Geometry, Image Acquisition Systems, Different types of digital images. Basic concepts of digital distances, distance transform, medial axis transform, component labeling, thinning, morphological processing, extension to gray scale morphology.

UNIT II IMAGE TRANSFORMS 9

1D DFT, 2D transforms - DFT, DCT, Discrete Sine, Walsh, Hadamard, Slant, Haar, KLT, SVD, Wavelet transform.

UNIT III SEGMENTATION OF GRAY LEVEL IMAGES 9

Histogram of gray level images, multilevel thresholding, Optimal thresholding using Bayesian classification, Watershed and Dam Construction algorithms for segmenting gray level image. Detection of edges and lines: First order and second order edge operators, multi-scale edge detection, Canny's edge detection algorithm, Hough transform for detecting lines and curves, edge linking.

UNIT IV IMAGE ENHANCEMENT AND COLOR IMAGE PROCESSING 9

Point processing, Spatial Filtering, Frequency domain filtering, multi-spectral image enhancement, image restoration. Color Representation, Laws of color matching, chromaticity diagram, color enhancement, color image segmentation, color edge detection, color demosaicing.

UNIT V IMAGE COMPRESSION 9

Lossy and lossless compression schemes, prediction based compression schemes, vector quantization, sub-band encoding schemes, JPEG compression standard, Fractal compression scheme, Wavelet compression scheme.

TOTAL : 45 PERIODS

OUTCOMES:

At the end of this course, the students should be able to:

- Discuss image enhancement techniques
- Explain color image processing
- Compare image compression schemes

REFERENCES:

1. A.K. Jain, “Fundamentals of Digital Image Processing”, Prentice-Hall, Addison-Wesley, 1989.
2. Bovik (ed.), “Handbook of Image and Video Processing”, Academic Press, 2000.
3. B. Jähne, “Practical Handbook on Image Processing for Scientific Applications“, CRC Press,1997.
4. Bernd Jähne, Digital Image Processing, Springer-Verlag Berlin Heidelberg 2005.
5. Gonzalez and Woods, Digital Image Processing, Prentice-Hall.
6. J. C. Russ. The Image Processing Handbook. CRC, Boca Raton, FL, 4th edn., 2002.
7. J. S. Lim, “Two-dimensional Signal and Image Processing” Prentice-Hall, 1990.
8. M. Petrou, P. Bosdogianni, “Image Processing, The Fundamentals“, Wiley, 1999.
9. Rudra Pratap, Getting Started With MATLAB 7. Oxford University Press, 2006
10. Stephane Marchand-Maillet, Yazid M. Sharaiha, Binary Digital Image Processing, A Discrete Approach, Academic Press, 2000
11. W. K. Pratt. Digital image processing, PIKS Inside. Wiley, New York, 3rd, edn., 2001.

VL5091 MEMS AND NEMS L T P C
3 0 0 3

OBJECTIVES:

- To introduce the concepts of microelectromechanical devices.
- To know the fabrication process of Microsystems.
- To know the design concepts of micro sensors and micro actuators.
- To familiarize concepts of quantum mechanics and nano systems.

UNIT I OVERVIEW 9

New trends in Engineering and Science: Micro and Nanoscale systems, Introduction to Design of MEMS and NEMS, MEMS and NEMS – Applications, Devices and structures. Materials for MEMS: Silicon, silicon compounds, polymers, metals.

UNIT II MEMS FABRICATION TECHNOLOGIES 9

Microsystem fabrication processes: Photolithography, Ion Implantation, Diffusion, Oxidation. Thin film depositions: LPCVD, Sputtering, Evaporation, Electroplating; Etching techniques: Dry and wet etching, electrochemical etching; Micromachining: Bulk Micromachining, Surface Micromachining, High Aspect- Ratio (LIGA and LIGA-like) Technology; Packaging: Microsystems packaging, Essential packaging technologies, Selection of packaging materials

UNIT III MICRO SENSORS 9

MEMS Sensors: Design of Acoustic wave sensors, resonant sensor, Vibratory gyroscope, Capacitive and Piezo Resistive Pressure sensors- engineering mechanics behind these Microsensors. Case study: Piezo-resistive pressure sensor.

UNIT IV MICRO ACTUATORS 9

Design of Actuators: Actuation using thermal forces, Actuation using shape memory Alloys, Actuation using piezoelectric crystals, Actuation using Electrostatic forces (Parallel plate, Torsion bar, Comb drive actuators), Micromechanical Motors and pumps. Case study: Comb drive actuators.

UNIT V NANOSYSTEMS AND QUANTUM MECHANICS 9

Atomic Structures and Quantum Mechanics, Molecular and Nanostructure Dynamics: Schrodinger Equation and Wave function Theory, Density Functional Theory, Nanostructures and Molecular Dynamics, Electromagnetic Fields and their quantization, Molecular Wires and Molecular Circuits.

TOTAL: 45 PERIODS

OUTCOMES:

At the end of this course, the student should be able to:

- Discuss micro sensors
- Explain micro actuators
- Outline nanosystems and Quantum mechanics

REFERENCES:

1. Chang Liu, "Foundations of MEMS", Pearson education India limited, 2006.
2. Marc Madou, "Fundamentals of Microfabrication", CRC press 1997.
3. Stephen D. Senturia," Micro system Design", Kluwer Academic Publishers,2001
4. Sergey Edward Lyshevski, "MEMS and NEMS: Systems, Devices, and Structures" CRC Press, 2002.
5. Tai Ran Hsu ,"MEMS and Microsystems Design and Manufacture" ,Tata Mcraw Hill, 2002.

VL5011 SCRIPTING LANGUAGES FOR VLSI L T P C
3 0 0 3

OBJECTIVES :

The students should be made to:

- Study scripting languages
- Understand security issues
- Learn concept of TCL phenomena

UNIT I INTRODUCTION TO SCRIPTING AND PERL 9

Characteristics of scripting languages, Introduction to PERL, Names and values, Variables and assignment, Scalar expressions, Control structures, Built-in functions, Collections of Data, Working with arrays, Lists and hashes, Simple input and output, Strings, Patterns and regular expressions, Subroutines, Scripts with arguments.

UNIT II ADVANCED PERL 9

Finer points of Looping, Subroutines, Using Pack and Unpack, Working with files, Navigating the file system, Type globs, Eval, References, Data structures, Packages, Libraries and modules, Objects, Objects and modules in action, Tied variables, Interfacing to the operating systems, Security issues.

UNIT III TCL 9

The TCL phenomena, Philosophy, Structure, Syntax, Parser, Variables and data in TCL, Control flow, Data structures, Simple input/output, Procedures, Working with Strings, Patterns, Files and Pipes, Example code.

UNIT IV ADVANCED TCL 9

The eval, source, exec and up-level commands, Libraries and packages, Namespaces, Trapping errors, Event-driven programs, Making applications 'Internet-aware', 'Nuts-and-bolts' internet programming, Security issues, running un trusted code, The C interface.

UNIT V TK AND JAVA SCRIPT 9

Visual tool kits, Fundamental concepts of TK, TK by example, Events and bindings, Geometry managers, PERL-TK. JavaScript – Object models, Design Philosophy, Versions of JavaScript, The Java Script core language, Basic concepts of Python. Object Oriented Programming Concepts (Qualitative Concepts Only): Objects, Classes, Encapsulation, Data Hierarchy.

TOTAL : 45 PERIODS

OUTCOMES:

At the end of this course, the students should be able to:

- Explain advanced TCL
- Discuss TK and Java script

REFERENCES:

1. Brent Welch,"Practical Programming in Tcl and Tk",Fourth Edition, 2003.
2. David Barron, "The World of Scripting Languages", Wiley Publications, 2000.
3. Guido van Rossum, and Fred L. Drake ", Python Tutorial, Jr., editor, Release 2.6.4
4. Randal L. Schwartz, "Learning PERL", Sixth Edition, O'Reilly.

AP5291 HARDWARE - SOFTWARE CO-DESIGN

L	T	P	C
3	0	0	3

OBJECTIVES:

- To acquire the knowledge about system specification and modelling.
- To learn the formulation of partitioning
- To study the different technical aspects about prototyping and emulation.

UNIT I SYSTEM SPECIFICATION AND MODELLING 9

Embedded Systems, Hardware/Software Co-Design, Co-Design for System Specification and Modeling , Co-Design for Heterogeneous Implementation - Single-Processor Architectures with one ASIC and many ASICs, Multi-Processor Architectures, Comparison of Co- Design Approaches, Models of Computation, Requirements for Embedded System Specification.

UNIT II HARDWARE / SOFTWARE PARTITIONING 9

The Hardware/Software Partitioning Problem, Hardware-Software Cost Estimation, Generation of the Partitioning Graph, Formulation of the HW/SW Partitioning Problem, Optimization, HW/SW Partitioning based on Heuristic Scheduling, HW/SW Partitioning based on Genetic Algorithms.

UNIT III HARDWARE / SOFTWARE CO-SYNTHESIS 9

The Co-Synthesis Problem, State-Transition Graph, Refinement and Controller Generation, Co-Synthesis Algorithm for Distributed System- Case Studies with any one application

UNIT IV PROTOTYPING AND EMULATION 9

Introduction, Prototyping and Emulation Techniques , Prototyping and Emulation Environments,Future Developments in Emulation and Prototyping ,Target Architecture- ArchitectureSpecialization Techniques ,System Communication Infrastructure, Target Architectures andApplication System Classes, Architectures for Control-Dominated Systems, Architectures forData-Dominated Systems ,Mixed Systems and Less Specialized Systems

UNIT V DESIGN SPECIFICATION AND VERIFICATION 9

Concurrency, Coordinating Concurrent Computations, Interfacing Components, Verification ,Languages for System-Level Specification and Design System-Level Specification ,Design Representation for System Level Synthesis, System Level Specification Languages, Heterogeneous Specification and Multi-Language Co- simulation.

TOTAL: 45 PERIODS

OUTCOMES:

- To assess prototyping and emulation techniques
- To compare hardware / software co-synthesis.
- To formulate the design specification and validate its functionality by simulation

REFERENCES:

1. Giovanni De Micheli , Rolf Ernst Morgon," Reading in Hardware/Software Co-Design" Kaufmann Publishers,2001.
2. Jorgen Staunstrup, Wayne Wolf ,"Hardware/Software Co-Design: Principles and Practice" , Kluwer Academic Pub,1997.
3. Ralf Niemann , "Hardware/Software Co-Design for Data Flow Dominated Embedded Systems", Kluwer Academic Pub, 1998.

VL5012 SELECTED TOPICS IN IC DESIGN L T P C
3 0 0 3

OBJECTIVES:

- This course deals with the supply circuit modules which are crucial modules in an IC design. Clock generation circuits play a major role in High Speed Broad Band Communication circuits, High Speed I/O's, Memory modules and Data Conversion Circuits.
- This course focuses on the design aspect of Clock Generation circuits and their design constraints.

UNIT I VOLTAGE AND CURRENT REFERENCES 9

Current Mirrors, Self Biased Current Reference, startup circuits, VBE based Current Reference, VT Based Current Reference, Band Gap Reference , Supply Independent Biasing, Temperature Independent Biasing, PTAT Current Generation, Constant Gm Biasing

UNIT II LOW DROP OUT REGULATORS 9

Analog Building Blocks, Negative Feedback, AC Design, Noise and Noise Reduction Techniques, Stability, LDO Efficiency, LDO Current Source, LDO Current Source Using Opamp.

UNIT III OSCILLATOR FUNDAMENTALS 9

General considerations, Ring oscillators, LC oscillators, Colpitts Oscillator, Jitter and Phase noise in Ring Oscillators, Impulse Sensitivity Function for Ring Oscillators, Phase Noise in Differential LC Oscillators.

UNIT IV PHASE LOCK LOOPS 9

PLL Fundamental, PLL stability, Noise Performance, Charge-Pump PLL Topology, CPPLL Building blocks, Jitter and Phase Noise performance.

UNIT V CLOCK AND DATA RECOVERY 9

CDR Architectures, Tias and Limiters, CMOS Interface, Linear Half Rate CMOS CDR Circuits, Wide capture Range CDR Circuits.

TOTAL: 45 PERIODS

OUTCOMES:

This course provides the essential know how to a designer to construct Supply reference circuits and Clock Generation Circuits for given design specifications and aids the designer to understand the design specifications related to Supply and Clock Generation Circuits.

REFERENCES:

1. BehzadRazavi, “ Design of Integrated circuits for Optical Communications”, McGraw Hill, 2003.
2. Floyd M. Gardner ,”Phase LocK Techniques” John wiley& Sons, Inc 2005.
3. Gabriel.A. Rincon-Mora, "Voltage references from diode to precision higher order bandgapcircuits”,Johnwiley& Sons, Inc 2002.
4. High Speed Clock and Data Recovery, High-performance Amplifiers Power Management “
5. springer, 2008.