PROGRAM EDUCATIONAL OBJECTIVES (PEOs)
1. To enable graduates to develop solutions to real world problems in the frontier areas of Applied Electronics.
2. To enable the graduates to adapt to the latest trends in technology through self-learning and to pursue research to meet out the demands in industries and Academia.
3. To enable the graduates to exhibit leadership skills and enhance their abilities through lifelong learning.

PROGRAM OUTCOMES (POs)

Engineering Graduates will be able to:

1. **Engineering knowledge**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

2. **Problem analysis**: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

3. **Design/development of solutions**: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

4. **Conduct investigations of complex problems**: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

5. **Modern tool usage**: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

6. **The engineer and society**: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

7. **Environment and sustainability**: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

8. **Ethics**: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

9. **Individual and team work**: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
10. **Communication**: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

11. **Project management and finance**: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one’s own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

12. **Life-long learning**: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

**PROGRAMME SPECIFIC OUTCOMES (PSOs)**

**PSO1**: To critically evaluate the design and provide optimal solutions to problem areas in advanced signal processing, digital system design, embedded systems and VLSI design.

**PSO2**: To enhance and develop electronic systems using modern engineering hardware and software tools.

**PSO3**: To work professionally and ethically in applied electronics and related areas.

Mapping of Programme Educational Objectives (PEOs) and the Program Outcomes (Pos):

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Mapping of Programme Specific Outcomes (PSOs) and the Program Outcomes (Pos):

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ANNA UNIVERSITY, CHENNAI  
AFFILIATED INSTITUTIONS  
M.E. APPLIED ELECTRONICS  
REGULATIONS – 2017  
CHOICE BASED CREDIT SYSTEM  
CURRICULA AND SYLLABI

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<td>CU5292</td>
<td>Electromagnetic Interference and Compatibility</td>
<td>PE</td>
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#### Semester II

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<td>1.</td>
<td>AP5003</td>
<td>VLSI Design Techniques</td>
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<td>Nano Electronics</td>
<td>PE</td>
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<td>Wireless Adhoc and Sensor Networks</td>
<td>PE</td>
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#### Semester II

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<td>1.</td>
<td>AP5072</td>
<td>DSP Architectures and Programming</td>
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<td>Speech and Audio Signal Processing</td>
<td>PE</td>
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<td>AP5092</td>
<td>Solid State Device Modeling and Simulation</td>
<td>PE</td>
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### SEMESTER III
#### ELECTIVE IV

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<td>CP5292</td>
<td>Internet of Things</td>
<td>PE</td>
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<td>System on Chip Design</td>
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<td>Robotics</td>
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<td>AP5006</td>
<td>Physical Design of VLSI Circuits</td>
<td>PE</td>
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### SEMESTER III
#### ELECTIVE V

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<th>P</th>
<th>C</th>
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<tr>
<td>1.</td>
<td>AP5094</td>
<td>Signal Integrity for High Speed Design</td>
<td>PE</td>
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<td>VL5091</td>
<td>MEMS and NEMS</td>
<td>PE</td>
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<td>AP5007</td>
<td>Secure Computing Systems</td>
<td>PE</td>
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<td>AP5008</td>
<td>Pattern Recognition</td>
<td>PE</td>
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</table>
MA5152  APPLIED MATHEMATICS FOR ELECTRONICS ENGINEERS  L T P C
4 0 0 4

OBJECTIVES:
The main objective of this course is to demonstrate various analytical skills in applied mathematics and extensive experience with the tactics of problem solving and logical thinking applicable in electronics engineering. This course also will help the students to identify, formulate, abstract, and solve problems in electrical engineering using mathematical tools from a variety of mathematical areas, including fuzzy logic, matrix theory, probability, dynamic programming and queuing theory.

UNIT I  FUZZY LOGIC  12
Classical logic – Multivalued logics – Fuzzy propositions – Fuzzy quantifiers.

UNIT II  MATRIX THEORY  12
Cholesky decomposition - Generalized Eigenvectors - Canonical basis - QR factorization - Least squares method - Singular value decomposition.

UNIT III  PROBABILITY AND RANDOM VARIABLES  12

UNIT IV  DYNAMIC PROGRAMMING  12

UNIT V  QUEUEING MODELS  12

TOTAL: 60 PERIODS

OUTCOMES:
After completing this course, students should demonstrate competency in the following skills:

- Concepts of fuzzy sets, knowledge representation using fuzzy rules, fuzzy logic, fuzzy prepositions and fuzzy quantifiers and applications of fuzzy logic.
- Apply various methods in matrix theory to solve system of linear equations.
- Computation of probability and moments, standard distributions of discrete and continuous random variables and functions of a random variable.
- Conceptualize the principle of optimality and sub-optimization, formulation and computational procedure of dynamic programming
- Exposing the basic characteristic features of a queuing system and acquire skills in analyzing queuing models.
- Using discrete time Markov chains to model computer systems.

REFERENCES:
OBJECTIVES:
- To introduce methods to analyze and design synchronous and asynchronous sequential circuits.
- To introduce the architectures of programmable devices.
- To introduce design and implementation of digital circuits using programming tools.

UNIT I  SEQUENTIAL CIRCUIT DESIGN
Analysis of clocked synchronous sequential circuits and modeling- State diagram, state table, state table assignment and reduction-Design of synchronous sequential circuits design of iterative circuits-ASM chart and realization using ASM

UNIT II ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN
Analysis of asynchronous sequential circuit – flow table reduction-races-state assignment-transition table and problems in transition table-design of asynchronous sequential circuit-Static, dynamic and essential hazards – data synchronizers – mixed operating mode asynchronous circuits – designing vending machine controller

UNIT III  FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS

UNIT IV SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES
Programming logic device families – Designing a synchronous sequential circuit using PLA/PAL – Realization of finite state machine using PLD – FPGA – Xilinx FPGA-Xilinx 4000

UNIT V SYSTEM DESIGN USING VERILOG

OUTCOMES:
At the end of the course, the student should be able to:
- Analyze and design sequential digital circuits
- Identify the requirements and specifications of the system required for a given application
- Design and use programming tools for implementing digital circuits of industry standards

REFERENCES:
OBJECTIVES:
- The student comprehends mathematical description and modelling of discrete time random signals.
- The student is conversant with important theorems and algorithms.
- The student learns relevant figures of merit such as power, energy, bias and consistency.
- The student is familiar with estimation, prediction and filtering concepts and techniques.

UNIT I DISCRETE RANDOM SIGNAL PROCESSING 9+6

UNIT II SPECTRUM ESTIMATION 9+6

UNIT III LINEAR ESTIMATION AND PREDICTION 9+6

UNIT IV ADAPTIVE FILTERS 9+6

UNIT V MULTIRATE DIGITAL SIGNAL PROCESSING 9+6

TOTAL 45+30: 75 PERIODS

OUTCOMES:
- Formulate time domain and frequency domain description of Wide Sense Stationary process in terms of matrix algebra and relate to linear algebra concepts.
- Explain various noise types, Yule-Walker algorithm, parametric and non-parametric methods, Wiener and Kalman filtering, LMS and RLS algorithms, Levinson Durbin algorithm, adaptive noise cancellation and adaptive echo cancellation, speed verses convergence issues, channel equalization, sampling rate change, subband coding and wavelet transform.
- Calculate mean, variance, auto-correlation and PSD for WSS stochastic processes, and derive prediction error criterion, Wiener-Hoff equations, Parseval's theorem,W-K theorem and normal equations.
- Design AR, MA, ARMA models, Weiner filter, anti aliasing and anti imaging filters, and develop FIR adaptive filter and polyphase filter structures.
- Simulate spectral estimation algorithms and basic models on computing platform.
REFERENCES:

AP5191 EMBEDDED SYSTEM DESIGN L T P C 3 0 0 3

OBJECTIVES:
The students should be made to:
- Learn design challenges and design methodologies
- Study general and single purpose processor
- Understand bus structures

UNIT I EMBEDDED SYSTEM OVERVIEW 9
Embedded System Overview, Design Challenges – Optimizing Design Metrics, Design Methodology, RT-Level Combinational and Sequential Components, Optimizing Custom Single-Purpose Processors.

UNIT II GENERAL AND SINGLE PURPOSE PROCESSOR 9
Basic Architecture, Pipelining, Superscalar and VLIW architectures, Programmer’s view, Development Environment, Application-Specific Instruction-Set Processors (ASIPs) Microcontrollers, Timers, Counters and watchdog Timer, UART, LCD Controllers and Analog-to-Digital Converters, Memory Concepts.

UNIT III BUS STRUCTURES 9

UNIT IV STATE MACHINE AND CONCURRENT PROCESS MODELS 9

UNIT V EMBEDDED SOFTWARE DEVELOPMENT TOOLS AND RTOS 9

TOTAL: 45 PERIODS
OUTCOMES:
At the end of this course, the students should be able to:
- Explain different protocols
- Discuss state machine and design process models
- Outline embedded software development tools and RTOS

REFERENCES:

AP5101 SENSORS, ACTUATORS AND INTERFACE ELECTRONICS L T P C
3 0 0 3

OBJECTIVES:
- Understand static and dynamic characteristics of measurement systems.
- Study various types of sensors.
- Study different types of actuators and their usage.
- Study State-of-the-art digital and semiconductor sensors.

UNIT I INTRODUCTION TO MEASUREMENT SYSTEMS 9
Introduction to measurement systems: general concepts and terminology, measurement systems, sensor classification, general input-output configuration, methods of correction, performance characteristics: static characteristics of measurement systems, accuracy, precision, sensitivity, other characteristics: linearity, resolution, systematic errors, random errors, dynamic characteristics of measurement systems: zero-order, first-order, and second-order measurement systems and response.

UNIT II RESISTIVE AND REACTIVE SENSORS 9
Resistive sensors: potentiometers, strain gages, resistive temperature detectors, magneto resistors, light-dependent resistors, Signal conditioning for resistive sensors: Wheatstone bridge, sensor bridge calibration and compensation, Instrumentation amplifiers, sources of interference and interference reduction, Reactance variation and electromagnetic sensors, capacitive sensors, differential, inductive sensors, linear variable differential transformers (LVDT), magneto elastic sensors, hall effect sensors, Signal conditioning for reactance-based sensors & application to the LVDT.

UNIT III SELF-GENERATING SENSORS 9

UNIT IV ACTUATORS DRIVE CHARACTERISTICS AND APPLICATIONS 9
Relays, Solenoid drive, Stepper Motors, Voice-Coil actuators, Servo Motors, DC motors and motor control, 4-to-20 mA Drive, Hydraulic actuators, variable transformers: synchros, resolvers, Inductosyn, resolver-to-digital and digital-to-resolver converters.
UNIT V DIGITAL SENSORS AND SEMICONDUCTOR DEVICE SENSORS

Digital sensors: position encoders, variable frequency sensors – quartz digital thermometer, vibrating wire strain gages, vibrating cylinder sensors, saw sensors, digital flow meters, Sensors based on semiconductor junctions: thermometers based on semiconductor junctions, magneto diodes and magneto transistors, photodiodes and phototransistors, sensors based on MOSFET transistors, CCD imaging sensors, ultrasonic sensors, fiber-optic sensors.

TOTAL: 45 PERIODS

OUTCOMES:
Upon completion of the course the student will be able to
- Compare Actuators
- Evaluate digital sensors and semiconductor device sensors
- Discuss Self-generating sensors

REFERENCES:

AP5111 ELECTRONICS SYSTEM DESIGN LABORATORY I

OBJECTIVES:
- To study of different interfaces
- To learn asynchronous and clocked synchronous sequential circuits
- To understand the concept of built in self test and fault diagnosis

2. Study of different interfaces ( using embedded microcontroller)
3. Implementation of Adaptive Filters and multistage multirate system in DSP Processor
4. Simulation of QMF using Simulation Packages
5. Analysis of Asynchronous and clocked synchronous sequential circuits
6. Built in self test and fault diagnosis
7. Sensor design using simulation tools
8. Design and analysis of real time signal processing system – Data acquisition and signal processing

TOTAL: 60 PERIODS
OUTCOMES:
Upon Completion of the course, the students will be able to:
- Apply PIC, MSP430, ‘51 Microcontroller and 8086 for system design
- Simulate QMF
- Design sensor using simulation tools
- Design and analyze of real time signal processing system

AP5251  SOFT COMPUTING AND OPTIMIZATION TECHNIQUES  L  T  P  C
3  0  0  3

OBJECTIVES:
- To learn various Soft computing frameworks.
- To familiarizes with the design of various neural networks.
- To understand the concept of fuzzy logic.
- To gain insight onto Neuro Fuzzy modeling and control.
- To gain knowledge in conventional optimization techniques.
- To understand the various evolutionary optimization techniques.

UNIT I  NEURAL NETWORKS  9
Machine Learning using Neural Network, Learning algorithms, Supervised Learning Neural Networks – Feed Forward Networks, Radial Basis Function, Unsupervised Learning Neural Networks – Self Organizing map, Adaptive Resonance Architectures, Hopfield network

UNIT II  FUZZY LOGIC  9

UNIT III  NEURO-FUZZY MODELING  9

UNIT IV  CONVENTIONAL OPTIMIZATION TECHNIQUES  9

UNIT V  EVOLUTIONARY OPTIMIZATION TECHNIQUES  9
Genetic algorithm - working principle, Basic operators and Terminologies, Building block hypothesis, Travelling Salesman Problem, Particle swarm optimization, Ant colony optimization.

TOTAL :45 PERIODS
OUTCOMES:
Upon Completion of the course, the students will be able to:
• Implement machine learning through Neural networks.
• Develop a Fuzzy expert system.
• Model Neuro Fuzzy system for clustering and classification.
• Able to use the optimization techniques to solve the real world problems

REFERENCES:

AP5252 ASIC AND FPGA DESIGN

OBJECTIVES:
• To study the design flow of different types of ASIC.
• To familiarize the different types of programming technologies and logic devices.
• To learn the architecture of different types of FPGA.
• To gain knowledge about partitioning, floor planning, placement and routing including circuit extraction of ASIC

UNIT I OVERVIEW OF ASIC AND PLD 9
Types of ASICs - Design flow – CAD tools used in ASIC Design – Programming Technologies: Antifuse – static RAM – EPROM and EEPROM technology, Programmable Logic Devices: ROMs and EPROMs – PLA –PAL. Gate Arrays – CPLDs and FPGAs

UNIT II ASIC PHYSICAL DESIGN 9
System partition -partitioning - partitioning methods – interconnect delay models and measurement of delay - floor planning - placement – Routing: global routing - detailed routing - special routing - circuit extraction - DRC

UNIT III LOGIC SYNTHESIS, SIMULATION AND TESTING 9
UNIT IV  FIELD PROGRAMMABLE GATE ARRAYS  

UNIT V  SOC DESIGN  

OUTCOMES:
- To analyze the synthesis, Simulation and testing of systems.
- To apply different high performance algorithms in ASICs.
- To discuss the design issues of SOC.

REFERENCES:

AP5291  HARDWARE - SOFTWARE CO-DESIGN  
OBJECTIVES:
- To acquire the knowledge about system specification and modelling.
- To learn the formulation of partitioning
- To study the different technical aspects about prototyping and emulation.

UNIT I  SYSTEM SPECIFICATION AND MODELLING

UNIT II  HARDWARE / SOFTWARE PARTITIONING
The Hardware/Software Partitioning Problem, Hardware-Software Cost Estimation, Generation of the Partitioning Graph, Formulation of the HW/SW Partitioning Problem, Optimization , HW/SW Partitioning based on Heuristic Scheduling, HW/SW Partitioning based on Genetic Algorithms.

UNIT III  HARDWARE / SOFTWARE CO-SYNTHESIS
The Co-Synthesis Problem, State-Transition Graph, Refinement and Controller Generation, Co-Synthesis Algorithm for Distributed System- Case Studies with any one application.
UNIT IV PROTOTYPING AND EMULATION  

UNIT V DESIGN SPECIFICATION AND VERIFICATION  

TOTAL: 45 PERIODS

OUTCOMES:
- To assess prototyping and emulation techniques
- To compare hardware / software co-synthesis.
- To formulate the design specification and validate its functionality by simulation

REFERENCES:

AP5292 DIGITAL IMAGE PROCESSING

OBJECTIVES:
The students should be made to:
- Understand fundamentals of digital images
- Learn different image transforms
- Study concept of segmentation

UNIT I DIGITAL IMAGE FUNDAMENTALS
A simple image model, Sampling and Quantization, Imaging Geometry, Digital Geometry, Image Acquisition Systems, Different types of digital images. Basic concepts of digital distances, distance transform, medial axis transform, component labeling, thinning, morphological processing, extension to gray scale morphology.

UNIT II IMAGE TRANSFORMS
1D DFT, 2D transforms - DFT, DCT, Discrete Sine, Walsh, Hadamard, Slant, Haar, KLT, SVD, Wavelet transform.
UNIT III  SEGMENTATION OF GRAY LEVEL IMAGES

Histogram of gray level images, multilevel thresholding, Optimal thresholding using Bayesian classification, Watershed and Dam Construction algorithms for segmenting gray level image. Detection of edges and lines: First order and second order edge operators, multi-scale edge detection, Canny’s edge detection algorithm, Hough transform for detecting lines and curves, edge linking.

UNIT IV  IMAGE ENHANCEMENT AND COLOR IMAGE PROCESSING

Point processing, Spatial Filtering, Frequency domain filtering, multi-spectral image enhancement, image restoration. Color Representation, Laws of color matching, chromaticity diagram, color enhancement, color image segmentation, color edge detection, color demosaicing.

UNIT V  IMAGE COMPRESSION

Lossy and lossless compression schemes, prediction based compression schemes, vector quantization, sub-band encoding schemes, JPEG compression standard, Fractal compression scheme, Wavelet compression scheme.

TOTAL: 45 PERIODS

OUTCOMES:
At the end of this course, the students should be able to:

- Discuss image enhancement techniques
- Explain color image processing
- Compare image compression schemes

REFERENCES:


AP5211  ELECTRONICS SYSTEM DESIGN LABORATORY II  L T P C

OBJECTIVES:

- To study of 32 bit ARM7 microcontroller RTOS and its application
- To understand testing RTOS environment and system programming
- To learn wireless network design using embedded systems
- To learn System design using ASIC
- To know use of Verilog and VHDL in sequential digital system modeling

20
1. Study of 32 bit ARM7 microcontroller RTOS and its application
2. Testing RTOS environment and system programming
3. Designing of wireless network using embedded systems
4. Implementation of ARM with FPGA
5. Design and Implementation of ALU in FPGA using VHDL and Verilog
6. Modeling of Sequential Digital system using Verilog and VHDL
7. Flash controller programming - data flash with erase, verify and fusing
8. System design using ASIC
9. Design, simulation and analysis of signal integrity

TOTAL: 60 PERIODS

OUTCOMES:
At the end of this course, the students should be able to:
- Utilize ARM with FPGA
- Demonstrate design of ALU in FPGA using VHDL and Verilog
- Assess flash controller programming - data flash with erase, verify and fusing
- Explain design, simulation and analysis of signal integrity

CP5281  TERM PAPER WRITING AND SEMINAR  L T P C
0 0 2 1

In this course, students will develop their scientific and technical reading and writing skills that they need to understand and construct research articles. A term paper requires a student to obtain information from a variety of sources (i.e., Journals, dictionaries, reference books) and then place it in logically developed ideas. The work involves the following steps:

1. Selecting a subject, narrowing the subject into a topic
2. Stating an objective.
3. Collecting the relevant bibliography (atleast 15 journal papers)
4. Preparing a working outline.
5. Studying the papers and understanding the authors contributions and critically analysing each paper.
6. Preparing a working outline
7. Linking the papers and preparing a draft of the paper.
8. Preparing conclusions based on the reading of all the papers.
9. Writing the Final Paper and giving final Presentation

Please keep a file where the work carried out by you is maintained.

Activities to be carried Out

<table>
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<th>Instructions</th>
<th>Submission week</th>
<th>Evaluation</th>
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<tr>
<td>Selection of area of interest</td>
<td>You are requested to select an area of interest, topic and</td>
<td>2&lt;sup&gt;nd&lt;/sup&gt; week</td>
<td>3 % Based on clarity of thought, current relevance and clarity in writing</td>
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<tr>
<td>and Topic</td>
<td>state an objective</td>
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<tr>
<td>Stating an Objective</td>
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</table>
| Collecting Information about your area & topic | 1. List 1 Special Interest Groups or professional society  
2. List 2 journals  
3. List 2 conferences, symposia or workshops  
4. List 1 thesis title  
5. List 3 web presences (mailing lists, forums, news sites)  
6. List 3 authors who publish regularly in your area  
7. Attach a call for papers (CFP) from your area. | 3rd week | 3% (the selected information must be area specific and of international and national standard) |
| --- | --- | --- | --- |
| Collection of Journal papers in the topic in the context of the objective – collect 20 & then filter | • You have to provide a complete list of references you will be using: Based on your objective -Search various digital libraries and Google Scholar  
• When picking papers to read - try to:  
  • Pick papers that are related to each other in some ways and/or that are in the same field so that you can write a meaningful survey out of them,  
  • Favour papers from well-known journals and conferences,  
  • Favour “first” or “foundational” papers in the field (as indicated in other people’s survey paper),  
  • Favour more recent papers,  
  • Pick a recent survey of the field so you can quickly gain an overview,  
  • Find relationships with respect to each other and to your topic area (classification scheme/categorization)  
  • Mark in the hard copy of papers whether complete work or section/sections of the paper are being considered. | 4th week | 6% (the list of standard papers and reason for selection) |
| Reading and notes for first 5 papers | Reading Paper Process  
• For each paper form a Table answering the following questions:  
  • What is the main topic of the article?  
  • What was/were the main issue(s) the author said they want to discuss?  
  • Why did the author claim it was important?  
  • How does the work build on other’s work, in the author’s opinion?  
  • What simplifying assumptions does the author claim to be making?  
  • What did the author do?  
  • How did the author claim they were going to evaluate their work and | 5th week | 8% (the table given should indicate your understanding of the paper and the evaluation is based on your conclusions about each paper) |
<table>
<thead>
<tr>
<th>Task Description</th>
<th>Process Description</th>
<th>Time Frame</th>
<th>Evaluation Criteria</th>
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<tbody>
<tr>
<td>Compare it to others?</td>
<td>- What did the author say were the limitations of their research?</td>
<td>6th week</td>
<td>8% (the table given should indicate your understanding of the paper and the evaluation is based on your conclusions about each paper)</td>
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<tr>
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<td>- What did the author say were the important directions for future research? Conclude with limitations/issues not addressed by the paper (from the perspective of your survey)</td>
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<tr>
<td>Reading and notes for next 5 papers</td>
<td>Repeat Reading Paper Process</td>
<td>6th week</td>
<td></td>
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<tr>
<td>Reading and notes for final 5 papers</td>
<td>Repeat Reading Paper Process</td>
<td>7th week</td>
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<tr>
<td>Draft outline 1 and Linking papers</td>
<td>Prepare a draft Outline, your survey goals, along with a classification / categorization diagram</td>
<td>8th week</td>
<td>8% (this component will be evaluated based on the linking and classification among the papers)</td>
</tr>
<tr>
<td>Abstract</td>
<td>Prepare a draft abstract and give a presentation</td>
<td>9th week</td>
<td>6% (Clarity, purpose and conclusion) 6% Presentation &amp; Viva Voce</td>
</tr>
<tr>
<td>Introduction Background</td>
<td>Write an introduction and background sections</td>
<td>10th week</td>
<td>5% (clarity)</td>
</tr>
<tr>
<td>Sections of the paper</td>
<td>Write the sections of your paper based on the classification / categorization diagram in keeping with the goals of your survey</td>
<td>11th week</td>
<td>10% (this component will be evaluated based on the linking and classification among the papers)</td>
</tr>
<tr>
<td>Your conclusions</td>
<td>Write your conclusions and future work</td>
<td>12th week</td>
<td>5% (conclusions – clarity and your ideas)</td>
</tr>
<tr>
<td>Final Draft</td>
<td>Complete the final draft of your paper</td>
<td>13th week</td>
<td>10% (formatting, English, Clarity and linking) 4% Plagiarism Check Report</td>
</tr>
<tr>
<td>Seminar</td>
<td>A brief 15 slides on your paper</td>
<td>14th &amp; 15th week</td>
<td>10% (based on presentation and Viva-Voce)</td>
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**TOTAL: 30 PERIODS**
OBJECTIVES:
- To familiarize about the features, specification and features of modern microprocessors.
- To gain knowledge about the architecture of Intel 32 and 64 bit microprocessors and salient features associated with them.
- To familiarize about the features, specification and features of modern microcontrollers.
- To gain knowledge about the 32 bit microcontrollers based on ARM and PIC32 architectures

UNIT I FEATURES OF MODERN MICROPROCESSORS

UNIT I HIGH PERFORMANCE CISC ARCHITECTURES
Introduction to IA 32 bit architecture – Intel Pentium Processors family tree – Memory Management – Branch prediction logic - Superscalar architecture – Hyper threading technology – 64 bit extension technology – Intel 64 bit architecture - Intel Core processor family tree – Turbo boost technology – Smart cache - features of Nehalem microarchitecture

UNIT II HIGH PERFORMANCE RISC ARCHITECTURE - ARM
RISC architecture merits and demerits – The programmer's model of ARM Architecture – 3-stage pipeline ARM organization - 3-stage pipeline ARM organization – ARM instruction execution – Salient features of ARM instruction set - ARM architecture profiles (A, R and M profiles)

UNIT III FEATURES OF MODERN MICROPROCESSORS
Introduction to microcontrollers – microcontroller vs microprocessors – microcontroller architecture - Processor Core – Memory interfaces - Communication interfaces (SPI, I²C, USB and CAN) – ADC - PWM – Watchdog timers – Interrupts – Debugging interfaces

UNIT IV HIGH PERFORMANCE MICROCONTROLLER ARCHITECTURES
Introduction to the Cortex-M Processor Family - ARM ‘Cortex-M3’ architecture for microcontrollers – Thumb 2 instruction technology – Internal Registers - Nested Vectored Interrupt controller - Memory map - Interrupts and exception handling – Applications of Cortex-M3 architecture

TOTAL : 45 PERIODS

OUTCOMES:
After completion of the course, the students should be able
- To explain the features and important specifications of modern microprocessors
- To explain the salient features CISC microprocessors based on IA-32 bit and IA-64 bit architectures
- To explain the salient features RISC processors based on ARM architecture and different application profiles of ARM core
- To explain the features and important specifications of modern microcontrollers
- To explain about ARM – M3 architecture and its salient features
REFERENCES:

AP5091 DIGITAL CONTROL ENGINEERING L T P C
3 0 0 3

OBJECTIVES:
- The student learns the principles of PI,PD,PID controllers.
- The student analyses time and frequency response discrete time control system.
- The student is familiar with digital control algorithms.
- The student has the knowledge to implement PID control algorithms.

UNIT I CONTROLLERS IN FEEDBACK SYSTEMS 9
Review of frequency and time response analysis and specifications of first order and second order feedback control systems, need for controllers, continuous time compensations, continuous time PI, PD, PID controllers, digital PID controllers.

UNIT II BASIC DIGITAL SIGNAL PROCESSING IN CONTROL SYSTEMS 9
Sampling theorem, quantization, aliasing and quantization error, hold operation, mathematical model of sample and hold, zero and first order hold, factors limiting the choice of sampling rate, reconstruction.

UNIT III MODELING OF SAMPLED DATA CONTROL SYSTEM 9
Difference equation description, Z-transform method of description, pulse transfer function, time and frequency response of discrete time control systems, stability of digital control systems, Jury’s stability test, state space description, first companion, second companion, Jordan canonical models, discrete state variable models (elementary principles only).

UNIT IV DESIGN OF DIGITAL CONTROL ALGORITHMS 9
Review of principle of compensator design, Z-plane specifications, digital compensator design using frequency response plots, discrete integrator, discrete differentiator, development of digital PID controller, transfer function, design in the Z-plane.

UNIT V PRACTICAL ASPECTS OF DIGITAL CONTROL ALGORITHMS 9
Algorithm development of PID control algorithms, standard programmes for microcontroller implementation, finite word length effects, choice of data acquisition systems, microcontroller based temperature control systems, microcontroller based motor speed control systems, DSP implementation of motor control system.

TOTAL: 45 PERIODS
OUTCOMES:
- Describe continuous time and discrete time controllers analytically.
- Define and state basic analog to digital and digital to analog conversion principles.
- Analyze sampled data control system in time and frequency domains.
- Design simple PI, PD, PID continuous and digital controllers.
- Develop schemes for practical implementation of temperature and motor control systems.

REFERENCES:

AP5001 COMPUTER ARCHITECTURE AND PARALLEL PROCESSING L T P C 3 0 0 3

OBJECTIVES:
- Understand the difference between pipeline and parallel processing concepts
- Study various types of processor architectures and the importance of scalable architectures
- Study Memory Architectures, Memory Technology and Optimization.


UNIT II PARALLEL PROCESSING, PIPELINING AND ILP 9 Instruction Level Parallelism and Its Exploitation - Concepts and Challenges - Pipelining processors - Overcoming Data Hazards with Dynamic Scheduling – Dynamic Branch Prediction - Speculation - Multiple Issue Processors - Performance and Efficiency in Advanced Multiple Issue Processors

UNIT III MEMORY HIERARCHY DESIGN 9 Memory Hierarchy - Memory Technology and Optimizations – Cache memory – Optimizations of Cache Performance – Memory Protection and Virtual Memory - Design of Memory Hierarchies.


TOTAL : 45 PERIODS
REFERENCES:

OBJECTIVES:
- To study various physical design methods in VLSI.
- To understand the concepts behind the VLSI design rules and routing techniques.
- To understand the concepts of various algorithms used for floor planning and routing techniques.

UNIT I INTRODUCTION TO VLSI DESIGN FLOW
Introduction to VLSI Design methodologies, Basics of VLSI design automation tools, Algorithmic Graph Theory and Computational Complexity, Tractable and Intractable problems, General purpose methods for combinatorial optimization.

UNIT II LAYOUT, PLACEMENT AND PARTITIONING
Layout Compaction, Design rules, Problem formulation, Algorithms for constraint graph compaction, Placement and partitioning, Circuit representation, Placement algorithms, Partitioning

UNIT III FLOOR PLANNING AND ROUTING
Floor planning concepts, Shape functions and floorplan sizing, Types of local routing problems, Area routing, Channel routing, Global routing, Algorithms for global routing.

UNIT IV SIMULATION AND LOGIC SYNTHESIS
Simulation, Gate-level modeling and simulation, Switch-level modeling and simulation, Combinational Logic Synthesis, Binary Decision Diagrams, Two Level Logic Synthesis.

UNIT V HIGH LEVEL SYNTHESIS
Hardware models for high level synthesis, internal representation, allocation, assignment and scheduling, scheduling algorithms, Assignment problem, High level transformations.

TOTAL: 45 PERIODS
REFERENCES:

CU5292 ELECTROMAGNETIC INTERFERENCE AND COMPATIBILITY L T P C 3 0 0 3

OBJECTIVES:
The students should be made to be familiar with:
- The basics of EMI
- EMI sources.
- EMI problems.
- Solution methods in PCB.
- Measurements techniques for emission.
- Measurement techniques for immunity.

UNIT I BASIC THEORY 9
Introduction to EMI and EMC, Intra and inter system EMI, Elements of Interference, Sources and Victims of EMI, Conducted and Radiated EMI emission and susceptibility, Case Histories, Radiation hazards to humans, Various issues of EMC, EMC Testing categories EMC Engineering Application.

UNIT II COUPLING MECHANISM 9
Electromagnetic field sources and Coupling paths, Coupling via the supply network, Common mode coupling, Differential mode coupling, Impedance coupling, Inductive and Capacitive coupling, Radioactive coupling, Ground loop coupling, Cable related emissions and coupling, Transient sources, Automotive transients.

UNIT III EMI MITIGATION TECHNIQUES 9
Working principle of Shielding and Murphy’s Law, LF Magnetic shielding, Apertures and shielding effectiveness, Choice of Materials for H, E, and free space fields, Gasketting and sealing, PCB Level shielding, Principle of Grounding, Isolated grounds, Grounding strategies for Large systems, Grounding for mixed signal systems, Filter types and operation, Surge protection devices, Transient Protection.

UNIT IV STANDARD AND REGULATION 9
UNIT V  EMI TEST METHODS AND INSTRUMENTATION

Fundamental considerations, EMI Shielding effectiveness tests, Open field test, TEM cell for immunity test, Shielded chamber, Shielded anechoic chamber, EMI test receivers, Spectrum analyzer, EMI test wave simulators, EMI coupling networks, Line impedance stabilization networks, Feed through capacitors, Antennas, Current probes, MIL-STD test methods, Civilian STD test methods.

TOTAL: 45 PERIODS

OUTCOMES:
At the end of this course, the student should be able to:
- Identify Standards
- Compare EMI test methods
- Discuss EMI mitigation techniques

REFERENCES:
5. Electromagnetic Compatibility by Norman Violette, Published by Springer, 2013

AP5003  VLSI DESIGN TECHNIQUES  L T P C
3 0 0 3

OBJECTIVES:
- This course deals comprehensively with all aspects of transistor level design of all the digital building blocks common to all CMOS microprocessors, DPSs, network processors, digital backend of all wireless systems etc.
- The focus will be on the transistor level design and will address all important issues related to size, speed and power consumption. The units are classified according to the important building and will introduce the principles and design methodology in terms of the dominant circuit choices, constraints and performance measures.

UNIT I  MOS TRANSISTOR PRINCIPLES AND CMOS INVERTER

MOS(FET) Transistor Characteristic under Static and Dynamic Conditions, MOS Transistor Secondary Effects, Process Variations, Technology Scaling, Internet Parameter and electrical wise models CMOS Inverter - Static Characteristic, Dynamic Characteristic, Power, Energy, and Energy Delay parameters.
UNIT II  COMBINATIONAL LOGIC CIRCUITS  9

UNIT III  SEQUENTIAL LOGIC CIRCUITS  9
Static Latches and Registers, Dynamic Latches and Registers, Timing Issues, Pipelines, Pulse and sense amplifier based Registers, Non bistable Sequential Circuits.

UNIT IV  ARITHMETIC BUILDING BLOCKS AND MEMORY ARCHITECTURES  9
Data path circuits, Architectures for Adders, Accumulators, Multipliers, Barrel Shifters, Speed and Area Tradeoffs, Memory Architectures, and Memory control circuits.

UNIT V  INTERCONNECT AND CLOCKING STRATEGIES  6

TOTAL : 45 PERIODS

OUTCOMES:
At the end of the course, the student should be able to:
• Carry out transistor level design of the most important building blocks used in digital CMOS VLSI circuits.
• Discuss design methodology of arithmetic building block
• Analyze tradeoffs of the various circuit choices for each of the building block.

REFERENCES:

AP5071  NANOELECTRONICS  L T P C
3 0 0 3

OBJECTIVES
• To understand how transistor as Nano device
• To understand various forms of Nano Devices
• To understand the Nano Sensors

UNIT I  SEMICONDUCTOR NANO DEVICES  9
Single-Electron Devices; Nano scale MOSFET – Resonant Tunneling Transistor - Single-Electron Transistors; Nanorobotics and Nanomanipulation; Mechanical Molecular Nanodevices; Nanocomputers: Optical Fibers for Nanodevices; Photochemical Molecular Devices; DNA-Based Nanodevices; Gas-Based Nanodevices.
UNIT II  ELECTRONIC AND PHOTONIC MOLECULAR MATERIALS

UNIT III  THERMAL SENSORS
Thermal energy sensors - temperature sensors, heat sensors - Electromagnetic sensors - electrical resistance sensors, electrical current sensors, electrical voltage sensors, electrical power sensors, magnetism sensors - Mechanical sensors - pressure sensors, gas and liquid flow sensors, position sensors - Chemical sensors - Optical and radiation sensors.

UNIT IV  GAS SENSOR MATERIALS
Criteria for the choice of materials - Experimental aspects – materials, properties, measurement of gas sensing property, sensitivity; Discussion of sensors for various gases, Gas sensors based on semiconductor devices.

UNIT V  BIOSENSORS
Principles - DNA based biosensors – Protein based biosensors – materials for biosensor applications - fabrication of biosensors - future potential.

OUTCOMES:
- To be able to simulate and design the nano device
- To be able to simulate and design the nano sensors

REFERENCES:
UNIT II ROUTING IN AD HOC NETWORKS

UNIT III MAC, ROUTING & QOS IN WIRELESS SENSOR NETWORKS

UNIT IV SENSOR MANAGEMENT

UNIT V SECURITY IN AD HOC AND SENSOR NETWORKS

TOTAL : 45 PERIODS

OUTCOMES:
Upon Completion of the course, the students should be able to
- Identify different issues in wireless ad hoc and sensor networks.
- To analyze protocols developed for ad hoc and sensor networks.
- To identify and address the security threats in ad hoc and sensor networks.
- Establish a Sensor network environment for different type of applications.

REFERENCES:
AP5004 HIGH PERFORMANCE NETWORKS

OBJECTIVES:
- To develop a comprehensive understanding of multimedia networking.
- To study the types of VPN and tunneling protocols for security.
- To learn about network security in many layers and network management.

UNIT I  INTRODUCTION

UNIT II  MULTIMEDIA NETWORKING APPLICATIONS
Streaming stored Audio and Video – Best effort service – protocols for real time interactive applications – Beyond best effort – scheduling and policing mechanism – integrated services – RSVP- differentiated services.

UNIT III  ADVANCED NETWORKS CONCEPTS

UNIT IV  TRAFFIC MODELLING
Little’s theorem, Need for modeling, Poisson modeling and its failure, Non- poisson models, Network performance evaluation.

UNIT V  NETWORK SECURITY AND MANAGEMENT

TOTAL: 45PERIODS

OUTCOMES:
Upon completion of this course, the students should be able to:
- Discuss advanced networks concepts
- Outline traffic modeling
- Evaluate network security

REFERENCES:
OBJECTIVES:
The objective of this course is to provide in-depth knowledge on
- Digital Signal Processor basics
- Third generation DSP Architecture and programming skills
- Advanced DSP architectures and some applications.

UNIT I  
FUNDAMENTALS OF PROGRAMMABLE DSPs 
Multiplier and Multiplier accumulator – Modified Bus Structures and Memory access in PDSPs – 
Multiple access memory – Multi-port memory – VLIW architecture- Pipelining – Special 
Addressing modes in P-DSPs – On chip Peripherals.

UNIT II  
SPECIAL FUNCTIONS
Architecture – Assembly language syntax - Addressing modes – Assembly language 
Instructions - Pipeline structure, Operation – Block Diagram of DSP starter kit – Application 
Programs for processing real time signals.

UNIT III  
LINEAR PROGRAMMING
Architecture of the C6x Processor - Instruction Set - DSP Development System: Introduction – 
DSP Starter Kit Support Tools- Code Composer Studio - Support Files - Programming 
Examples to Test the DSK Tools – Application Programs for processing real time signals.

UNIT IV  
ALGEBRAIC EQUATIONS
Architecture of ADSP-21XX and ADSP-210XX series of DSP processors- Addressing modes 
and assembly language instructions – Application programs –Filter design, FFT calculation.

UNIT V  
ORDINARY DIFFERENTIAL EQUATIONS
Architecture of TMS320C54X: Pipe line operation, Code Composer studio – Architecture of 
TMS320C6X - Architecture of Motorola DSP563XX – Comparison of the features of DSP family 
processors.

TOTAL : 45 PERIODS

OUTCOMES:
Students should be able to:
- Become Digital Signal Processor specialized engineer
- DSP based System Developer

REFERENCES:
Microprocessors with Examples from TMS320C54xx, cengage Learning India Private 
Limited, Delhi 2012
2. B.Venkataramani and M.Bhaskar, “Digital Signal Processors – Architecture, 
New Delhi, 2003.
3. RulphChassaing, Digital Signal Processing and Applications with the C6713 and 
C6416 DSK, A JOHN WILEY & SONS, INC., PUBLICATION, 2005
OBJECTIVES:
- The CMOS RF Front End (RFE) is a very crucial building block and in all of wireless and many high frequency wire-line systems. The RFE has few important building blocks within including the Low Noise Amplifiers, Phase Locked Loop Synthesizers, Mixers, Power Amplifiers, and impedance matching circuits.
- The present course will introduce the principles of operation and design principles associated with these important blocks.
- The course will also provide and highlight the appropriate digital communication related design objectives and constraints associated with the RFEs

UNIT I CMOS PHYSICS, TRANSCEIVER SPECIFICATIONS AND ARCHITECTURES
Introduction to MOSFET Physics, Noise: Thermal, shot, flicker, popcorn noise, Two port Noise theory, Noise Figure, THD, IP2, IP3, Sensitivity, SFDR, Phase noise - Specification distribution over a communication link, Homodyne Receiver, Heterodyne Receiver, Image reject, Low IF Receiver Architectures Direct upconversion Transmitter, Two step upconversion Transmitter.

UNIT II IMPEDANCE MATCHING AND AMPLIFIERS
S-parameters with Smith chart, Passive IC components, Impedance matching networks, Common Gate, Common Source Amplifiers, OC Time constants in bandwidth estimation and enhancement, High frequency amplifier design, Power match and Noise match, Single ended and Differential LNAs, Terminated with Resistors and Source Degeneration LNAs.

UNIT III FEEDBACK SYSTEMS AND POWER AMPLIFIERS
Stability of feedback systems: Gain and phase margin, Root-locus techniques, Time and Frequency domain considerations, Compensation, General model – Class A, AB, B, C, D, E and F amplifiers, Power amplifier Linearisation Techniques, Efficiency boosting techniques, ACPR metric, Design considerations.

UNIT IV MIXERS AND OSCILLATORS
Mixer characteristics, Non-linear based mixers, Quadratic mixers, Multiplier based mixers, Single balanced and double balanced mixers, subsampling mixers, Oscillators describing Functions, Colpitts oscillators Resonators, Tuned Oscillators, Negative resistance oscillators, Phase noise.

UNIT V PLL AND FREQUENCY SYNTHESIZERS
Linearised Model, Noise properties, Phase detectors, Loop filters and Charge pumps, Integer-N frequency synthesizers, Direct Digital Frequency synthesizers.

TOTAL : 45 PERIODS

OUTCOMES:
- The student after completing this course must be able to translate the top level wireless communications system specifications into block level specifications of the RFE.
- The student should be also able to carry out transistor level design of the entire RFE.

REFERENCES:
4. Recorded lectures and notes available at . http://www.ee.iitm.ac.in/~ani/ee6240/
OBJECTIVES:
- To study basic concepts of processing speech and audio signals
- To study and analyse various M-band filter-banks for audio coding
- To understand audio coding based on transform coders.
- To study time and frequency domain speech processing methods

UNIT I  MECHANICS OF SPEECH AND AUDIO  9

UNIT II  TIME-FREQUENCY ANALYSIS: FILTER BANKS AND TRANSFORMS  9
Introduction - Analysis-Synthesis Framework for M-band Filter Banks- Filter Banks for Audio Coding: Design Considerations - Quadrature Mirror and Conjugate Quadrature Filters - Tree-Structured QMF and CQF M-band Banks - Cosine Modulated “Pseudo QMF” M-band Banks -Cosine Modulated Perfect Reconstruction (PR) M-band Banks and the Modified Discrete Cosine Transform (MDCT) - Discrete Fourier and Discrete Cosine Transform - Pre-echo Distortion- Pre-echo Control Strategies

UNIT III  AUDIO CODING AND TRANSFORM CODERS  9

UNIT IV  TIME AND FREQUENCY DOMAIN METHODS FOR SPEECH PROCESSING  9

UNIT V  PREDICTIVE ANALYSIS OF SPEECH  9

OUTCOMES:
Upon completion of this course, the students should be able to:
- Evaluate audio coding and transform coders
- Discuss time and frequency domain methods for speech processing
- Explain predictive analysis of speech
REFERENCES:

AP5092 SOLID STATE DEVICE MODELLING AND SIMULATION

OBJECTIVES:
- To understand the concept of device modeling
- To learn multistep method
- To study device simulations

UNIT I MOSFET DEVICE PHYSICS MOSFET
capacitor, Basic operation, Basic modeling, Advanced MOSFET modeling, RF modeling of MOS transistors, Equivalent circuit representation of MOS transistor, High frequency behavior of MOS transistor and A.C small signal modeling, model parameter extraction, modeling parasitic BJT, Resistors, Capacitors, Inductors.

UNIT II DEVICE MODELLING
Prime importance of circuit and device simulations in VLSI; Nodal, mesh, modified nodal and hybrid analysis equations. Solution of network equations: Sparse matrix techniques, solution of nonlinear networks through Newton-Raphson technique, convergence and stability.

UNIT III MULTISTEP METHODS
Solution of stiff systems of equations, adaptation of multistep methods to the solution of electrical networks, general purpose circuit simulators.

UNIT IV MATHEMATICAL TECHNIQUES DEVICE SIMULATIONS
Poisson equation, continuity equation, drift-diffusion equation, Schrodinger equation, hydrodynamic equations, trap rate, finite difference solutions to these equations in 1D and 2D space, grid generation.

UNIT V SIMULATION OF DEVICES
Computation of characteristics of simple devices like p-n junction, MOS capacitor and MOSFET; Small-signal analysis.

TOTAL : 45 PERIODS

OUTCOMES:
Upon completion of this course, the students should be able to:
- Explain the importance of MOS Capacitor and Small signal modeling
- Apply and determine the drift diffusion equation and stiff system equation.
- Analyze circuits using parasitic BJT parameters and newton Raphson method.
- Model the MOS transistor using schrodinger equation and Multistep methods.
REFERENCES:

CP5292  INTERNET OF THINGS  L T P C
3  0  0  3

OBJECTIVES:
- To understand the fundamentals of Internet of Things
- To learn about the basics of IOT protocols
- To build a small low cost embedded system using Raspberry Pi.
- To apply the concept of Internet of Things in the real world scenario

UNIT I  INTRODUCTION TO IoT  9
Internet of Things - Physical Design- Logical Design- IoT Enabling Technologies - IoT Levels & Deployment Templates - Domain Specific IoTs - IoT and M2M - IoT System Management with NETCONF-YANG- IoT Platforms Design Methodology

UNIT II  IoT ARCHITECTURE  9
M2M high-level ETSI architecture - IETF architecture for IoT - OGC architecture - IoT reference model - Domain model - information model - functional model - communication model - IoT reference architecture

UNIT III  IoT PROTOCOLS  9

UNIT IV  BUILDING IoT WITH RASPBERRY PI & ARDUINO  9

UNIT V  CASE STUDIES AND REAL-WORLD APPLICATIONS  9
Real world design constraints - Applications - Asset management, Industrial automation, smart grid, Commercial building automation, Smart cities - participatory sensing - Data Analytics for IoT – Software & Management Tools for IoT Cloud Storage Models & Communication APIs - Cloud for IoT - Amazon Web Services for IoT.

TOTAL :45 PERIODS
OUTCOMES:
Upon completion of this course, the students should be able to:
- Analyze various protocols for IoT
- Develop web services to access/control IoT devices.
- Design a portable IoT using Raspberry Pi
- Deploy an IoT application and connect to the cloud.
- Analyze applications of IoT in real time scenario

REFERENCES:

UNIT I INTRODUCTION
Introduction to SoC Design, system level design, methodologies and tools, system hardware: IO, communication, processing units, memories; operating systems: prediction of execution, real time scheduling, embedded OS, middleware; Platform based SoC design, multiprocessor SoC and Network on Chip, Low power SoC Design

UNIT II SYSTEM LEVEL MODELLING
SystemC: overview, Data types, modules, notion of time, dynamic process, basic channels, structure communication, ports and interfaces, Design with examples

UNIT III HARDWARE SOFTWARE CO-DESIGN
Analysis, partitioning, high level optimisations, real-time scheduling, hardware acceleration, voltage scaling and power management; Virtual platform models, co-simulation and FPGAs for prototyping of HW/SW systems.

UNIT IV SYNTHESIS
System synthesis: Transaction Level Modelling (TLM) based design, automatic TLM generation and mapping, platform synthesis; software synthesis: code generation, multi task synthesis, internal and external communication; Hardware synthesis: RTL architecture, Input models, estimation and optimisation, resource sharing and pipelining and scheduling
UNIT V  SOC VERIFICATION AND TESTING

SoC and IP integration, Verification : Verification technology options, verification methodology, overview: system level verification, physical verification, hardware/software co-verification; Test requirements and methodologies, SoC design for testability - System modeling, test power dissipation, test access mechanism

TOTAL : 45 PERIODS

OUTCOMES:
- Analyse algorithms and architecture of hardware software inorder to optimise the system based on requirements and implementation constraints
- Model and specify systems at high level of abstraction
- appreciate the co-design approach and virtual platform models
- Understand hardware, software and interface synthesis

REFERENCES
3. Erik Larson, Introduction to advanced system-on-chip test design and optimisation, Springer 2005

AP5093  ROBOTICS

OBJECTIVES:
- To understand robot locomotion and mobile robot kinematics
- To understand perception in robotics
- To understand mobile robot localization
- To understand mobile robot mapping
- To understand simultaneous localization and mapping (SLAM)
- To understand robot planning and navigation
UNIT I  LOCOMOTION AND KINEMATICS  9
Introduction to Robotics – key issues in robot locomotion – legged robots – wheeled mobile robots –
aerial mobile robots – introduction to kinematics – kinematics models and constraints – robot
maneuverability

UNIT II  ROBOT PERCEPTION  9
Sensors for mobile robots – vision for robotics – cameras – image formation – structure from stereo –
structure from motion – optical flow – color tracking – place recognition – range data

UNIT III  MOBILE ROBOT LOCALIZATION  9
Introduction to localization – challenges in localization – localization and navigation – belief
representation – map representation – probabilistic map-based localization – Markov localization –
EKF localization – UKF localization – Grid localization – Monte Carlo localization – localization in
dynamic environments

UNIT IV  MOBILE ROBOT MAPPING  9
Autonomous map building – occupancy grip mapping – MAP occupancy mapping – SLAM –extended
Kalman Filter SLAM – graph-based SLAM – particle filter SLAM – sparse extended
information filter – fastSLAM algorithm.

UNIT V  PLANNING AND NAVIGATION  9
Introduction to planning and navigation – planning and reacting – path planning – obstacle
avoidance techniques – navigation architectures – basic exploration algorithms

TOTAL 45 PERIODS

OUTCOMES:
Upon Completion of the course, the students will be able to
• Explain robot locomotion
• Apply kinematics models and constraints
• Implement vision algorithms for robotics
• Implement robot localization techniques
• Implement robot mapping techniques
• Implement SLAM algorithms
• Explain planning and navigation in robotics

REFERENCES:
2. Howie Choset et al., “Principles of Robot Motion: Theory, Algorithms, and
4. Roland Seigwart, Illah Reza Nourbaksh, and Davide Scaramuzza, “Introduction to
5. Sebastian Thrun, Wolfram Burgard, and Dieter Fox, “Probabilistic Robotics”, MIT
OBJECTIVES:
- To introduce the physical design concepts such as routing, placement, partitioning and packaging
- To study the performance of circuits layout designs, compaction techniques.

UNIT I INTRODUCTION TO VLSI TECHNOLOGY

UNIT II PLACEMENT USING TOP-DOWN APPROACH

UNIT III ROUTING USING TOP DOWN APPROACH

UNIT IV PERFORMANCE ISSUES IN CIRCUIT LAYOUT

UNIT V SINGLE LAYER ROUTING, CELL GENERATION AND COMPACTION

TOTAL: 45 PERIODS

OUTCOMES:
Upon Completion of the course, the students will be able to
- Explain different types of routing
- Discuss performance issues in circuit layout
- Outline 1D compaction- 2D compaction.

REFERENCES:
OBJECTIVES:
- To identify sources affecting the speed of digital circuits.
- To introduce methods to improve the signal transmission characteristics.

UNIT I SIGNAL PROPAGATION ON TRANSMISSION LINES
Transmission line equations, wave solution, wave vs. circuits, initial wave, delay time, Characteristic impedance, wave propagation, reflection, and bounce diagrams Reactive terminations – L, C, static field maps of micro strip and strip line cross-sections, per unit length parameters, PCB layer stackups and layer/Cu thicknesses, cross-sectional analysis tools, Zo and Td equations for microstrip and stripline Reflection and terminations for logic gates, fan-out, logic switching, input impedance into a transmission-line section, reflection coefficient, skin-effect, dispersion.

UNIT II MULTI-CONDUCTOR TRANSMISSION LINES AND CROSS-TALK
Multi-conductor transmission-lines, coupling physics, per unit length parameters, Near and far-end cross-talk, minimizing cross-talk (stripline and microstrip) Differential signalling, termination, balanced circuits, S-parameters, Lossy and Lossless models.

UNIT III NON-IDEAL EFFECTS
Non-ideal signal return paths – gaps, BGA fields, via transitions, Parasitic inductance and capacitance, Transmission line losses – Rs, tanδ, routing parasitic, Common-mode current, differential-mode current, Connectors.

UNIT IV POWER CONSIDERATIONS AND SYSTEM DESIGN
SSN/SSO, DC power bus design, layer stack up, SMT decoupling, Logic families, power consumption, and system power delivery, Logic families and speed Package types and parasitic, SPICE, IBIS models, Bit streams, PRBS and filtering functions of link-path components, Eye diagrams, jitter, inter-symbol interference, Bit-error rate, Timing analysis.

UNIT V CLOCK DISTRIBUTION AND CLOCK OSCILLATORS
Timing margin, Clock slew, low impedance drivers, terminations, Delay Adjustments, canceling parasitic capacitance, Clock jitter.

OUTCOMES:
- Ability to identify sources affecting the speed of digital circuits.
- Able to improve the signal transmission characteristics.

REFERENCES:

TOOLS REQUIRED
1. SPICE, source - http://www-cad.eecs.berkeley.edu/Software/software.html
OBJECTIVES:
- To introduce the concepts of microelectromechanical devices.
- To know the fabrication process of Microsystems.
- To know the design concepts of micro sensors and micro actuators.
- To familiarize concepts of quantum mechanics and nano systems.

UNIT I OVERVIEW
9

UNIT II MEMS FABRICATION TECHNOLOGIES
9

UNIT III MICRO SENSORS
9
MEMS Sensors: Design of Acoustic wave sensors, resonant sensor, Vibratory gyroscope, Capacitive and Piezo Resistive Pressure sensors- engineering mechanics behind these Microsensors. Case study: Piezo-resistive pressure sensor.

UNIT IV MICRO ACTUATORS
9

UNIT V NANOSYSTEMS AND QUANTUM MECHANICS
9
Atomic Structures and Quantum Mechanics, Molecular and Nanostructure Dynamics: Schrodinger Equation and Wave function Theory, Density Functional Theory, Nanostructures and Molecular Dynamics, Electromagnetic Fields and their quantization, Molecular Wires and Molecular Circuits.

TOTAL: 45 PERIODS

OUTCOMES:
At the end of this course, the student should be able to:
- Discuss micro sensors
- Explain micro actuators
- Outline nanosystems and Quantum mechanics

REFERENCES:
AP5007  SECURE COMPUTING SYSTEMS  L  T  P  C
3  0  0  3

OBJECTIVES:
• To learn computer hardware, system software and data concepts from a security perspective

UNIT I  COMPUTER SECURITY AND MANAGEMENT  9

UNIT II  HARDWARE SECURITY  9

UNIT III  ASSEMBLY AND OPERATING SYSTEMS SECURITY  9
Opcode, Operands, Addressing Modes, Stack and Buffer Overflow, FIFO and M/M/1 Problem, Kernel, Drivers and OS Security; Secure Design Principles, Trusted Operating Systems, Trusted System Functions

UNIT IV  ADVANCED COMPUTER ARCHITECTURE  9
Security aspects: Multiprocessors, parallel processing, Ubiquitous computing, Grid, Distributed and cloud computing, Internet computing, Virtualization

UNIT V  NETWORK AND WEBSECURITY  9
TCP/IP Protocol, Network switches, Routers, Gateways, Wireless Networks and Network Address Translation (NAT); Network Security Issues in TCP/IP, Threat Models, Denial of Service Attacks, Firewalls, Intrusion Detection, Browser Attacks, Web Attacks Targeting Users, Email Attacks, Secure Shell (SSH), HTTPS

TOTAL : 45 PERIODS

OUTCOMES:
• Aware of Security aspects
• Able to appreciate security in hardware, OS and its future need
• Learn security issues in various types of computing networks

REFERENCES:
OBJECTIVES:

- To learn about supervised and unsupervised pattern classifiers.
- To familiarize about different feature extraction techniques.
- To explore the role of Hidden Markov model and SVM in pattern recognition.
- To understand the application of Fuzzy logic and genetic algorithms for pattern classifier.

UNIT I  PATTERN CLASSIFIER


UNIT II  CLUSTERING

Clustering for unsupervised learning and classification – Clustering concept – C Means algorithm – Hierarchical clustering – Graph theoretic approach to pattern Clustering – Validity of Clusters.

UNIT III  FEATURE EXTRACTION AND STRUCTURAL PATTERN RECOGNITION

Principal component analysis, Independent component analysis, Linear discriminant analysis, Feature selection through functional approximation – Elements of formal grammars, Syntactic description – Stochastic grammars – Structural Representation.

UNIT IV  HIDDEN MARKOV MODELS AND SUPPORT VECTOR MACHINE


UNIT V  RECENT ADVANCES

Fuzzy logic – Fuzzy Pattern Classifiers – Pattern Classification using Genetic Algorithms – Case Study Using Fuzzy Pattern Classifiers and Perception.

TOTAL: 45 PERIODS

OUTCOMES:

Upon completion of the course the student will be able to

- Differentiate between supervised and unsupervised classifiers
- Classify the data and identify the patterns.
- Extract feature set and select the features from given data set.
- Apply fuzzy logic and genetic algorithms for classification problems.

REFERENCES:
